

Apr. 2025



SCB18X128XX0AF

128Mbit DDR OPI Xccela PSRAM
EU RoHS Compliant Products

Data Sheet

Rev. I

Revision History		
Date	Revision	Subjects (major changes since last revision)
2022-12-08	A	1. P4 IDD spec done 2. Marketing want Ron 250ohm, based on Bailu, Ron max is 240ohm, need to discuss
2023-02-02	B	1. Table 6, RL 400MHZ and 333MHZ changed 2. Table 8, Vendor ID update 3. Figure 16 & 18, A3 A0 A0 A0 change to A3 A2 A1 A0 4. P4 & P25 TC extend from 105°C to 125°C 5. Update 1.2 Table 1 6. Remove Table 20 Note
2023-03-14	C	1. Table 1 update part number 2. P4 operation temperature using extended range 2 and extended range 1 3. Table 24 tCEM using extended temp2 and extended temp1 to satisfy retention 4. Table 20 operation condition add extended temp 2 and temp 1 5. Table 22 & Table 23 IDD items added based on temperature
2023-03-28	D	1. Table 6, RL 400MHZ and 333MHZ changed back to v0.1 for same RL and WL
2023-06-27	E	1. P4 update IDD; 2. P15 change Read variable description and Clock toggle suggestion; 3. Figure7 – Figure10, Figure13 correct read DQ preamble and tHZ; 4. Table21 – Table22 update IDD value; 5. Remove RBX description; 6. Add MR8[5] bit description; 7. Add MR0[6] bit description; 8. Update MR6 description; 9. Remove the clock stop recommend in Read/Write; 10. Add note of tCSP/tCHD for clock not stop during CE_n High; 11. Correct some spell mistakes.
2023-09-6	F	1. Fill the blanks in IDD table with TBD; 2. Fill the TBD values in AC timing table; 3. Update table 1 part number 4. Change feature Tj to Tc, and change standard temperature range 5. Package ballout remove x8 and notes
2024-07-31	G	1. Adding Figure 2 Package Outline Drawing 2. Adding part number for component
2024-08-22	H	1. Update IDD value of Table 23 2. Update description and value of ISB _{STDDPD} in Table 23 3. Update ISB _{EXT1} / ISB _{EXT2} / ISB _{STDroom} value of Table23 4. Update Note4/ Note5 of Table23 3. Add Note6 of Table23 4. Update typical value of Table21/Table22 5. Update IDD values of 1.1 Features 6. Update tCPH & tDQSK
2025-04-09	I	1. Remove DPD

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1 Overview

This chapter gives an overview of the 128Mbit PSRAM component product and describes its main characteristics.

1.1 Features

Specifications

- Single Supply Voltage
 - VDD=1.8V, VDDmin=1.62V, VDDmax= 1.98V
 - VDDQ=1.8V, VDDQmin=1.62V, VDDQmax= 1.98V
- Interface
 - two Bytes transfers per clock cycle in x8 mode
 - two Words transfer per clock cycle in x16 mode
 - Mode register configurable x8(default) / x16 mode
- Max. clock rate: 400MHz
- Max. data rate: 800MBps for DDR mode -- x8
1600MBps for DDR mode -- x16
- Organization: 128Mb in x8 mode(default)
 - 16M x 8bits, 128Mb;
 - Column address: CA0~CA10;
 - Row address: RA0~RA12
 - Page size: 2048 Bytes
- Organization: 128Mb in x16 mode
 - 8M x 16bits, 128Mb;
 - Column address: CA0~CA9;
 - Row address: RA0~RA12
 - Page size: 1024 Words
- Refresh: auto-managed
- Operation Temperature
 - Tc = -25°C ~ +85°C (standard range)
 - Tc = -40°C ~ +105°C (extended range 2)
 - Tc = -40°C ~ +125°C (extended range 1)
- Typical mean Room Standby Current
 - 53uA @ 25°C
 - 22uA @ 25°C(Half Sleep Mode with data retained)
- Maximum Standby Current
 - 68uA @ 25°C

Features

- Low Power Feature
 - Partial Array Self-Refresh (PASR)
 - Auto Temperature Compensated Self-Refresh
 - Configurable refresh rate
 - Half Sleep Mode with data retained
- Software Reset
- LVCMOS output driver with programmable drive strength
- Support Write Data Mask
- High speed read operation with Data Strobe
- Register Configurable write and read initial latencies
- Burst length
 - max. 2048 Bytes(x8) / 1024 Word(x16)
 - min. 2 Bytes(x8) / 2 Words(x16)
- Wrap & Hybrid Burst
 - 16/32/64/2K Bytes length in x8 mode
 - 16/32/64/1K Words length in x16 mode
- Linear Burst Command
- Optional host control of refresh rate via MR0[7]
- x16 mode can be configured by setting MR8[6] = 1(default is x8 mode and MR8[6] = 0)

1.2 Product List

Table 1 shows all possible products within the 128Mbit PSRAM generation. Availability depends on application needs.

Table 1 - Ordering Information for 128Mbit PSRAM

Part Number	IO	Temperature Range	Max Frequency	Note
SCB18X128800AF-10E	x8	Tc= -25°C ~ +85°C	400MHz	miniBGA 24L
SCB18X128160AF-10E	x16	Tc= -25°C ~ +85°C	400MHz	miniBGA 24L
SCB18X128800AF-10E2	x8	Tc= -40°C ~ +105°C	400MHz	miniBGA 24L
SCB18X128160AF-10E2	x16	Tc= -40°C ~ +105°C	400MHz	miniBGA 24L
SCB18X128800AF-10E1	x8	Tc= -40°C ~ +125°C	400MHz	miniBGA 24L
SCB18X128160AF-10E1	x16	Tc= -40°C ~ +125°C	400MHz	miniBGA 24L
SCB18X128160AF-05E2	x16	Tc= -40°C ~ +105°C	200MHz	miniBGA 24L

1.3 PSRAM Addressing

Table 2 - 128Mbit PSRAM Addressing

Configuration	16M × 8bits	8M x 16bits	Note
Internal Organization	16M × 8bits	8M × 16bits	
Row Address	A[12:0]	A[12:0]	
Number of addressable Rows	8K	8K	
Column Address	A[10:0]	A[9:0]	
Number of addressable Columns (page length)	2048	1024	1)
Page Size	2K Bytes	1K Words	2)

Note:

- 1) Page length is the number of addressable columns and is defined as 2^{COLBITS} , where COLBITS is the number of column address bits.
- 2) Page size is the number of bytes of data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered.

Octal DDR PSRAM device is byte-addressable(x8) / word-addressable(x16). PSRAM accesses are required to start on even addresses (A[0]='0). Mode Register accesses allow both even and odd addresses.

1.4 Package Ballout

The PSRAM is available in miniBGA 24L package, the Figure 1 is PSRAM Ballout for 128Mb components

Figure 1 - PSRAM Ballout for 128Mb components

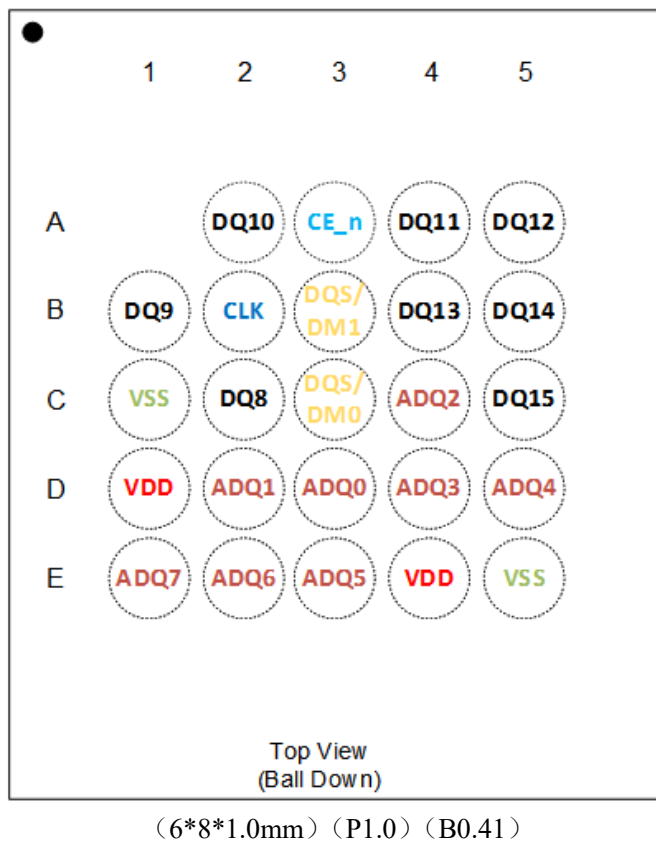
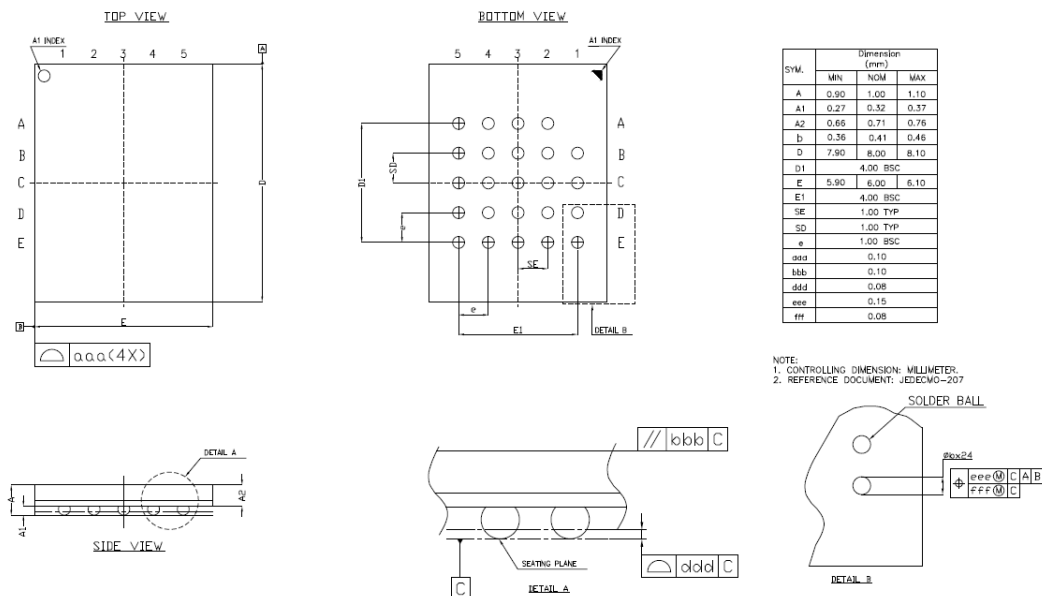


Figure 2 - Package Outline Drawing



1.5 Input / Output Signal Functional Description

Table 3 - Input / Output Signal Functional Description

Symbol	Type	Function	Comments
VDD	Supply	Core & IO power supply 1.8V	VDDQ short to VDD internally
VSS	Supply	Core & IO supply ground	
A/DQ[7:0]	IO	Address and DQ bus[7:0]	used in x8 and x16 mode
DQ[15:8]	IO	DQ bus[15:8]	used in x16 mode only
DQS/DM[0]	IO	DQ strobe clock for DQ[7:0] during all reads, Data mask for DQ[7:0] during memory writes, DM is active, DM =1 means “do not write”	used in x8 and x16 mode
DQS/DM[1]	IO	DQ strobe clock for DQ[15:8] during all reads, Data mask for DQ[15:8] during memory writes, DM is active, DM =1 means “do not write”	used in x16 mode only
CE_n	Input	Chip select, active low. When CE_n=1, chip is in standby state.	
CLK	Input	Clock	
RESET_n	Input	Reset signal, active low, optional as the pad is internally tied to a weak Pull-up and can be left floating	May not be available for all package types

2 Functional Description

2.1 Command Truth Tables

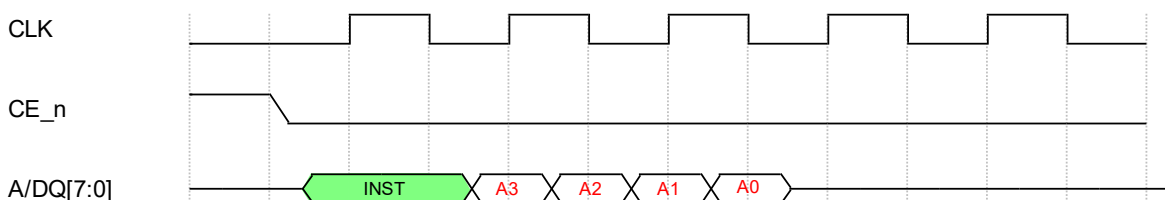
The truth tables list the input signal values at a given clock edge which represent a command or state transition expected to be executed by the PSRAM. Table 4 lists all valid commands to the PSRAM.

Table 4- Command Truth Table

Function	1 st CLK		2 nd CLK		3 rd CLK	
	rising edge	falling edge	rising edge	falling edge	rising edge	falling edge
Sync Read	00h		A3	A2	A1	A0
Sync Write	80h		A3	A2	A1	A0
Sync Read (Linear Burst)	20h		A3	A2	A1	A0
Sync Write (Linear Burst)	A0h		A3	A2	A1	A0
Mode Register Read	40h		V			MA
Mode Register Write	C0h		V			MA
Global Reset	FFh		V			
NOTE1 “V” means “H or L (but a defined logic level)”						
NOTE2 A3 = 8*bx unused address bits are reserved and should remain 0						
NOTE3 A2 = RA[12:5]						
NOTE4 A1 = RA[4:0], CA[10:8], CA[10] is used only in x8 mode						
NOTE5 A0 = CA[7:0]						
NOTE6 MA= Mode Register Address						
NOTE7 The linear burst commands, 20h and A0h, ignore burst setting defined by MR8[2:0]						
NOTE8 It is strongly recommended to disable clock(keep low) when CE_n is high						

As shown in Figure 2, after CE_n goes LOW, instruction code is latched on 1st CLK rising edge. Access address is latched on the 3rd, 4th, 5th & 6th CLK edges (2nd CLK rising edge, 2nd CLK falling edge, 3rd CLK rising edge, 3rd CLK falling edge).

Figure 3 - Command and Address latch



2.2 Mode Register

Seven groups of Mode Registers are defined to control various operating modes of PSRAM. Shown in Table 5

Table 5- Mode Register Table

MR num	MA[7:0]	READ/ WRITE	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	`h00	R/W	TSO	Drive Str ext	LT	Read Latency Code			Drive Str.	
1	`h01	R	ULP	RFU		Vendor ID				
2	`h02	R	KGD			Dev ID		Density		
3	`h03	R	0	0	SRF		RFU			
4	`h04	R/W	Write Latency Code			RF		PASR		
6	`h06	W	Half Sleep							
8	`h08	R/W	0	x8/x16	High freq. enable	RFU	0	BT	BL	

Table 6- MR0 Mode register Definition

Field	Bits	Description																																																																																				
Drive Str	OP[1:0]	Output Drive Strength codes. Combined with MR0[6]. If MR0[6] = 0: 00B Full (25Ω default) 01B Half (50Ω) 10B 1/4 (100Ω) 11B 1/8 (200Ω) If MR0[6] = 1: Output Drive Strength resistor extended by about 1.2 times compare with MR0[6]=0 only when MR0[1:0] =11B. When MR0[1:0] is not 11B, the MR0[6] is unused.																																																																																				
Read Latency Code	OP[4:2]	Read latency is related with Read Latency Type(OP[5]). Read latency is pushed out up to LCx2 when internal Refresh is ongoing. <table><tr><th></th><th></th><th colspan="2">VL Codes (MR0[5]=0)</th><th>FL Codes (MR0[5]=1)</th><th colspan="2">Max. Input CLK Freq (MHz)</th></tr><tr><th>MR8[5]</th><th>MR0[4:2]</th><th>Latency (LC)</th><th>Max push out (LCx2)</th><th>Latency (LCx2)</th><th>Standard</th><th>Extended</th></tr><tr><td>0B</td><td>000B</td><td>3</td><td>6</td><td>6</td><td>66</td><td>66</td></tr><tr><td>0B</td><td>001B</td><td>4</td><td>8</td><td>8</td><td>109</td><td>109</td></tr><tr><td>0B</td><td>010B</td><td>5(default)</td><td>10</td><td>10</td><td>133</td><td>133</td></tr><tr><td>0B</td><td>011B</td><td>6</td><td>12</td><td>12</td><td>166</td><td>166</td></tr><tr><td>0B</td><td>100B</td><td>7</td><td>14</td><td>14</td><td>200</td><td>200</td></tr><tr><td>0B</td><td>101B</td><td>8</td><td>16</td><td>16</td><td>225</td><td>225</td></tr><tr><td>0B</td><td>110B</td><td>9</td><td>18</td><td>18</td><td>250</td><td>250</td></tr><tr><td>0B</td><td>111B</td><td>11</td><td>22</td><td>22</td><td>300</td><td>300</td></tr><tr><td>1B</td><td>000B</td><td>12</td><td>24</td><td>24</td><td>333</td><td>333</td></tr><tr><td>1B</td><td>001B</td><td>16</td><td>32</td><td>32</td><td>400</td><td>400</td></tr></table>			VL Codes (MR0[5]=0)		FL Codes (MR0[5]=1)	Max. Input CLK Freq (MHz)		MR8[5]	MR0[4:2]	Latency (LC)	Max push out (LCx2)	Latency (LCx2)	Standard	Extended	0B	000B	3	6	6	66	66	0B	001B	4	8	8	109	109	0B	010B	5(default)	10	10	133	133	0B	011B	6	12	12	166	166	0B	100B	7	14	14	200	200	0B	101B	8	16	16	225	225	0B	110B	9	18	18	250	250	0B	111B	11	22	22	300	300	1B	000B	12	24	24	333	333	1B	001B	16	32	32	400	400
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0B	010B	5(default)	10	10	133	133																																																																																
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1B	000B	12	24	24	333	333																																																																																
1B	001B	16	32	32	400	400																																																																																
Read Latency Type	OP[5]	0B Variable (default) 1B Fixed																																																																																				
Drive Strength extend	OP[6]	Extend driver strength of 200Ohm; Details in MR0[1:0].																																																																																				
Temperature Sensor Override	OP[7]	0B On-die thermal sensor controls refresh rate according to MR4[4:3](default). 1B Force refresh rate set by MR4[4:3].(Host takes on role of on-die built-in thermal sensor)																																																																																				

Table 7– Operation Latency Code

Type	Operation	VL (default)		FL
		No Refresh	Refresh	
Memory	Read	LC	Up to LCx2	LCx2
	Write	WLC		WLC
Register	Read	LC		LC
	Write	1		1

Table 8– MR1 Mode register Definition

Field	Bits	Description
Vendor ID	OP[4:0]	11010: UNIIC
Ultra Low Power Device mapping	OP[7]	0B Non-ULP (no Half Sleep) 1B ULP (Half Sleep supported)

Table 9– MR2 Mode register Definition

Field	Bits	Description
Device Density mapping	OP[2:0]	001B 32Mb 011B 64Mb 101B 128Mb(default) 111B 256Mb others reserved
Device ID	OP[4:3]	00B Version A(default) 01B Version B 10B Version C 11B Version D
Good-Die Bit	OP[7:5]	110B PASS others FAIL Note: Default is FAIL die, and only mark PASS after all test passed.

Table 10– MR3 Mode register Definition

Field	Bits	Description
Self Refresh Flag	OP[5:4]	MR3[5:4] indicates current device refresh rate. Refresh rate depends on temperature and refresh frequency configuration. Set by MR4[4:3]. 01B 0.5x Refresh 00B 1x Refresh 10B 4x Refresh 11B reserved

Table 11– MR4 Mode register Definition

Field	Bits	Description																																													
PASR	OP[2:0]	If PASR (Partial Array Self-Refresh) is enabled, only data located in the specified areas of the array will be refreshed. This feature can reduce standby current.																																													
		128Mb x8 (MR8[6] = 0B default) address space RA[12:0],CA[10:0]																																													
		<table><tr><th>Codes</th><th>Refresh Coverage</th><th>Address Space</th><th>Size</th><th>Density</th></tr><tr><td>000B</td><td>Full array (default)</td><td>000000h-FFFFFFh</td><td>16M x8</td><td>128Mb</td></tr><tr><td>001B</td><td>Bottom 1/2 array</td><td>000000h-7FFFFFFh</td><td>8M x8</td><td>64Mb</td></tr><tr><td>010B</td><td>Bottom 1/4 array</td><td>000000h-3FFFFFFh</td><td>4M x8</td><td>32Mb</td></tr><tr><td>011B</td><td>Bottom 1/8 array</td><td>000000h-1FFFFFFh</td><td>2M x8</td><td>16Mb</td></tr><tr><td>100B</td><td>None</td><td>0</td><td>0M</td><td>0Mb</td></tr><tr><td>101B</td><td>Top 1/2 array</td><td>800000h-FFFFFFh</td><td>8M x8</td><td>64Mb</td></tr><tr><td>110B</td><td>Top 1/4 array</td><td>C00000h-FFFFFFh</td><td>4M x8</td><td>32Mb</td></tr><tr><td>111B</td><td>Top 1/8 array</td><td>E00000h-FFFFFFh</td><td>2M x8</td><td>16Mb</td></tr></table>	Codes	Refresh Coverage	Address Space	Size	Density	000B	Full array (default)	000000h-FFFFFFh	16M x8	128Mb	001B	Bottom 1/2 array	000000h-7FFFFFFh	8M x8	64Mb	010B	Bottom 1/4 array	000000h-3FFFFFFh	4M x8	32Mb	011B	Bottom 1/8 array	000000h-1FFFFFFh	2M x8	16Mb	100B	None	0	0M	0Mb	101B	Top 1/2 array	800000h-FFFFFFh	8M x8	64Mb	110B	Top 1/4 array	C00000h-FFFFFFh	4M x8	32Mb	111B	Top 1/8 array	E00000h-FFFFFFh	2M x8	16Mb
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		111B	Top 1/8 array	700000h-7FFFFFFh	1M x16	16Mb																																									
		Note: CA[10] is ignored in x16 mode.																																													
		Refresh Frequency	OP[4:3]	x0B Always 4x Refresh(default)																																											
				01B Enables 1x Refresh when temperature allows																																											
11B Enable 0.5x Refresh when temperature allows																																															
Note: x = don't care																																															
Write Latency	OP[7:5]	Write latency, WLC, default to 5 after power up																																													
		Write Latency Code contain MR4[7:5] and MR8[5]																																													
		<table><tr><th>MR8[5]</th><th>MR4[7:5]</th><th>Write Latency</th><th>Fmax (MHz)</th></tr><tr><td>0B</td><td>000B</td><td>3</td><td>66</td></tr><tr><td>0B</td><td>100B</td><td>4</td><td>109</td></tr><tr><td>0B</td><td>010B</td><td>5(default)</td><td>133</td></tr><tr><td>0B</td><td>110B</td><td>6</td><td>166</td></tr><tr><td>0B</td><td>001B</td><td>7</td><td>200</td></tr><tr><td>0B</td><td>101B</td><td>8</td><td>225</td></tr><tr><td>0B</td><td>011B</td><td>9</td><td>250</td></tr><tr><td>0B</td><td>111B</td><td>11</td><td>300</td></tr><tr><td>1B</td><td>000B</td><td>12</td><td>333</td></tr><tr><td>1B</td><td>100B</td><td>16</td><td>400</td></tr></table>	MR8[5]	MR4[7:5]	Write Latency	Fmax (MHz)	0B	000B	3	66	0B	100B	4	109	0B	010B	5(default)	133	0B	110B	6	166	0B	001B	7	200	0B	101B	8	225	0B	011B	9	250	0B	111B	11	300	1B	000B	12	333	1B	100B	16	400	
		MR8[5]	MR4[7:5]	Write Latency	Fmax (MHz)																																										
		0B	000B	3	66																																										
		0B	100B	4	109																																										
		0B	010B	5(default)	133																																										
		0B	110B	6	166																																										
		0B	001B	7	200																																										
		0B	101B	8	225																																										
		0B	011B	9	250																																										
		0B	111B	11	300																																										
		1B	000B	12	333																																										
		1B	100B	16	400																																										

Table 12– MR6 Mode register Definition

Field	Bits	Description
HSM	OP[7:0]	11110000B Half Sleep mode others reserved

Table 13– MR8 Mode register Definition

Field	Bits	Description				
Burst Length	OP[1:0]	The device is power up in 32 Bytes(x8) / 32 Words(x16) Hybrid Wrap, however, non-hybrid burst and other burst length can be set by MR8[2:0]. Minimum write and read burst length is 2 bytes(x8) / words(x16). And no restriction on maximum burst length as long as tCEM is met.				
Burst Type	OP[2]	MR8[2]	MR8[1:0]	Burst Length	Example of Sequence of Bytes During Wrap	
					Starting Address	Byte Sequence
		0B	00B	16 Byte/Word Wrap	4	[4,5,6,...15,0,1,2,...]
		0B	01B	32 Byte/Word Wrap	4	[4,5,6,...31,0,1,2,...]
		0B	10B	64 Byte/Word Wrap	4	[4,5,6,...63,0,1,2,...]
		0B	11B	2K Byte/ 1K Word Wrap	4	[4,5,6,...2047,0,1,2,...]
		1B	00B	16 Byte/Word Hybrid Wrap	2	[2,3,...15,0,1],16,17,...2047,0,1,...
		1B	01B	32 Byte/Word Hybrid Wrap (default)	2	[2,3,...31,0,1],32,33,...2047,0,1,...
		1B	10B	64 Byte/Word Hybrid Wrap	2	[2,3,...63,0,1],64,65,...2047,0,1,...
		1B	11B	2K Byte/1K word Wrap	2	[2,3,...2047,0,1,2,...]
High Freq. Enable	OP[5]	High frequency latency enable for 333Mhz and 400Mhz.				
x8/x16 mode selectable	OP[6]	0B device power up in x8 mode (default) 1B device power up in x16 mode Device power up in x8 mode. After power up device can be configured to x16 mode by setting MR8[6]=1 via MRW. Host can switch in and out of x16 mode any time after power up.				

The Linear Burst Write or Read Command (INST[7:0] = A0H or INST[7:0] = 20H) can forces the current array write / read command to do 2K Bytes in x8 mode or 1K Words in x16 mode Wrap (equivalent to having MR8[1:0] set to 2'b11). The burst command write / read linearly from the starting address and wrap back to the beginning of the page upon reaching the end of page. To access a different page, host must issue a new command.

2.3 Power-Up Initialization

There is an internal voltage detector to start the automatic initialization process. VDD and VDDQ must be applied simultaneously. When they reach a stable level at or above minimum VDD, the device is in Phase 1 and will require 150 μ s to complete its auto-initialization process. The user can then proceed to Phase 2 of the initialization described in this section.

During Phase 1 CE_n should remain HIGH (track VDD within 200mV); CLK should remain LOW.

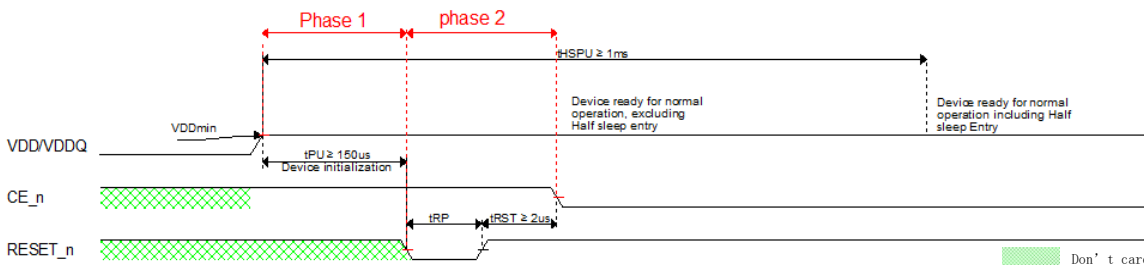
After Phase 2 is complete the device is ready for operation, however Half Sleep entry are not available until Half Sleep Power Up (tHSPU) duration is observed.

There are two method for Power-Up Initialization, By RESET_n pin or by the reset command.

- **Power-Up Initialization by RESET_n pin**

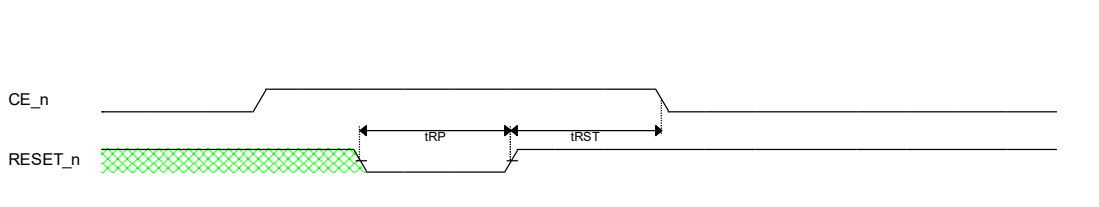
The RESET_n pin can be used to initialize the device during Phase 2 as follows Figure 3:

Figure 4 - Power-up Initialization with RESET_n pin



The RESET_n pin can also be used at any time after the device is initialized to reset all register contents. Memory content is not guaranteed after reset. Timing requirements for RESET_n usage are shown below Figure 4:

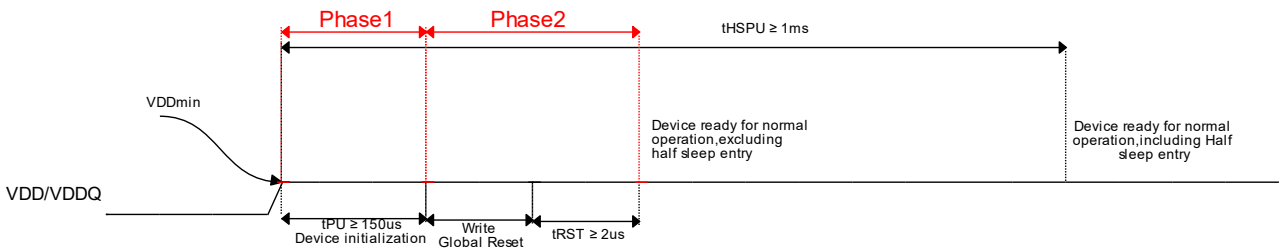
Figure 5 - Reset_n pin Timing



- **Power-Up Initialization by Global Reset command**

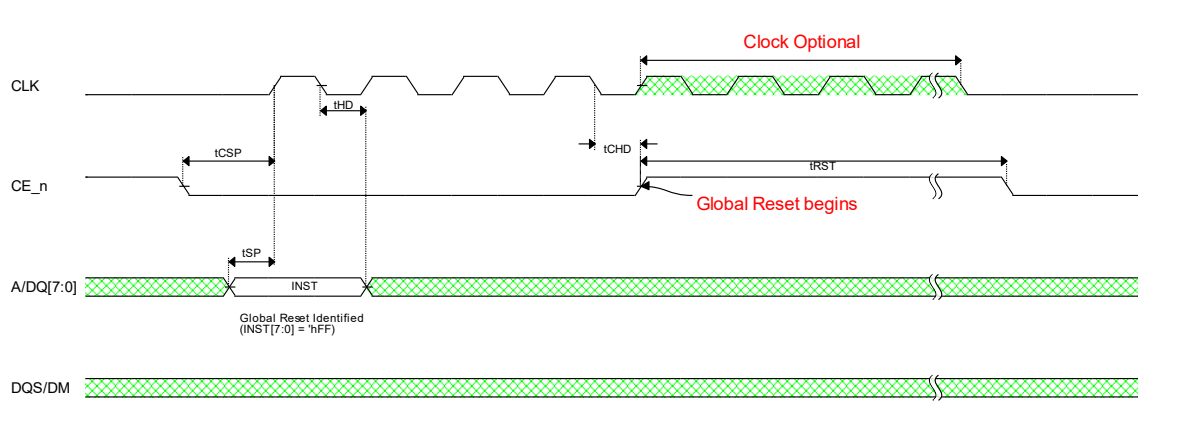
As an alternate power-up initialization method, After the Phase 1 150 μ s period the Global Reset command is used to reset the device in Phase 2 as follows Figure 5:

Figure 6 - Power-Up Initialization with Global Reset command



The Global Reset command resets all register contents. Memory content is not guaranteed. The command frame is made of 4 clocked CE# lows. Clocking is optional during tRST. The Global Reset command sequence is shown below Figure 6.

Figure 7 - Global Reset command



2.4 Read

After address latching, the device drive DQS/DM to 0 from next CLK rising edge of the 3rd clock cycle (A1). See Figure 7 below.

Output data is available after Read Latency cycles, as shown in Figure8 & Figure9. Read Latency is defined in MR0[5:2] and MR8[5]. When data is valid, A/DQ[7:0] and DQS/DM follow the timing specified in Figure 10. Synchronous timing parameters are shown in Table 24 & Table 25.

In case of internal refresh insertion, variable latency output data may be delayed by **up to** (LCx2) latency cycles as shown in Figure 9. True variable refresh push out latency can be anywhere **between** LC to LCx2. The 1st DQS/DM rising edge after read pre-amble indicates the beginning of valid data.

In x16 mode DQ[15:8] will not receiver INST/ADD, instead they will remain Hi-Z until read latency and then start pumping out data, similar to DQ[7:0].

Figure 8 - Synchronous Read

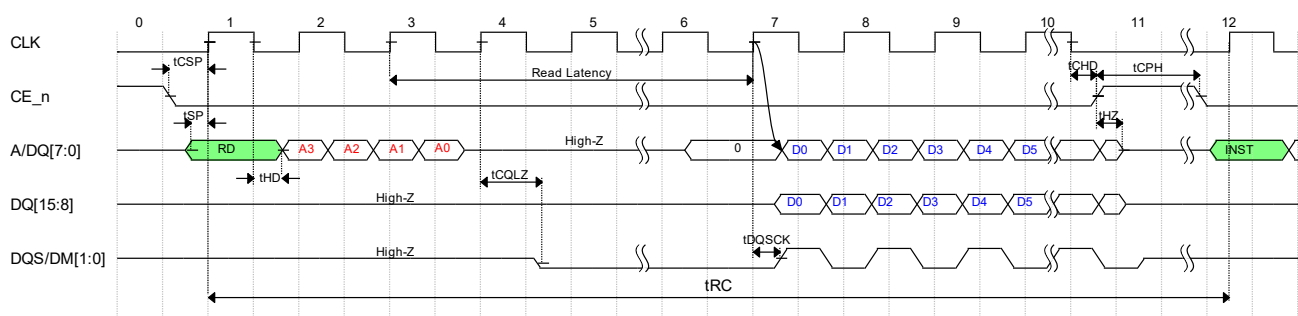


Figure 9 - Synchronous Read without internal refresh

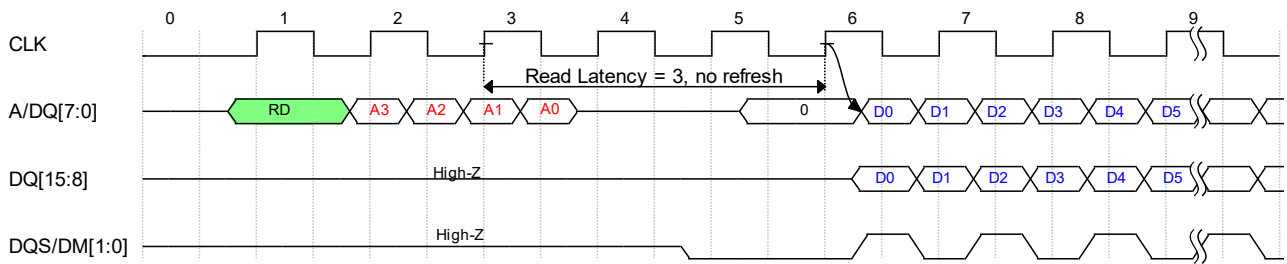


Figure 10 - Synchronous Read with internal refresh

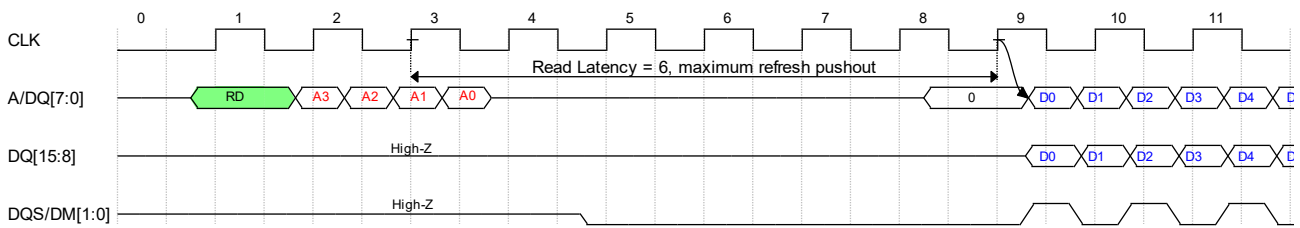
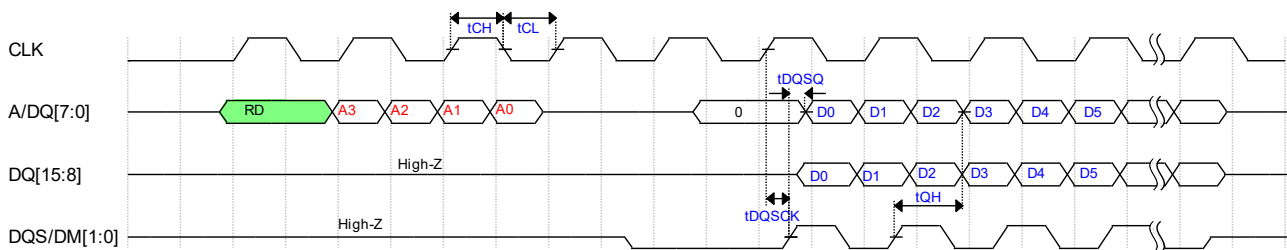


Figure 11 - Read DQS/DM & DQ timing



Note:

- 1) All DQ are valid tDQSQ after the DQS edge, regardless of tDQSK
- 2) DQS/DM[1] is DQS/DM for DQ[15:8], DQS/DM[0] is DQS/DM for DQ[7:0]

2.5 Write

At least 2 bytes(in x8 mode) / 2 words(in x16 mode) of data must be input in a write operation. For short burst writes tRC must be met, and for long burst writes, tCEM must be met. During write data input DQS/DM is used to mask the corresponding write data, DQS/DM low means the write data is valid and will be written into array, DQS/DM high means the write data is mask as shown in figure 11.

In x16 mode, DQ[15:8] are ignored during INST/ADDR cycles, instead, DQ[15:8] are only used after write latency to receive the data, similar to DQ[7:0], During write data cycle the DQ[15:8] and DQ[7:0] can be independently masked via DM[1] and DM[0].

Figure 12 - Synchronous Write

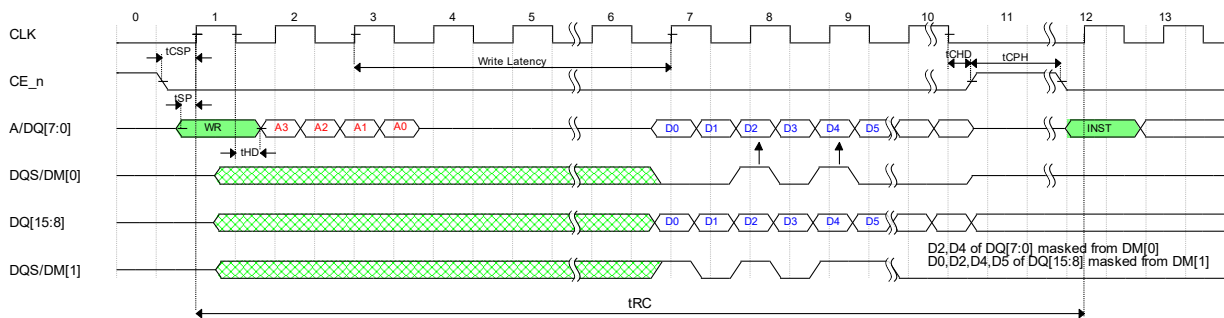
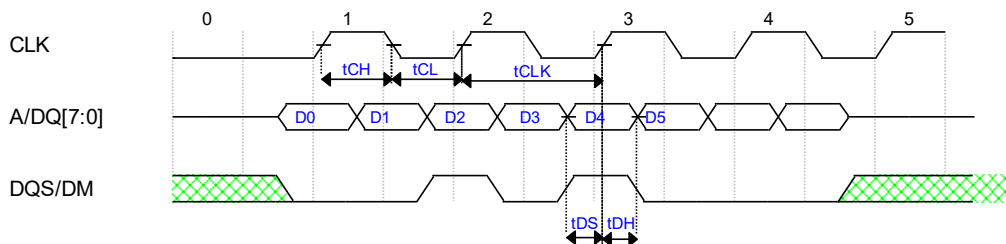


Figure 12 shows the write timing, tDS/tDH are the DQ and DM setup/hold time relates to CLK.

Figure 13 - Write Timing



Note: DQS/DM[1] is DQS/DM for DQ[15:8], DQS/DM[0] is DQS/DM for DQ[7:0]

2.6 Mode Register Read/Write

All mode registers are 8-bit wide, mode register read and write uses only A/DQ[7:0] and DQS/DM[0] even in x16 mode.

● Mode Register Read

Mode Register Read latency defines in 'Table 7 – Operation Latency Code', no push out by internal refresh, As shown in Figure 13, MA indicates which Mode Register content will be read out.

Figure 14 - Mode Register Read

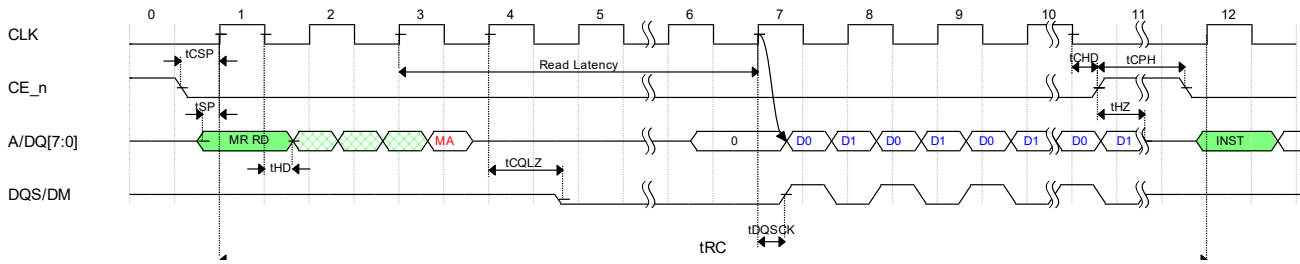


Table 14 shows the relationship of MA and the read out MR data.

Table 14— MA decoder for MR read

MA	D0	D1
0	MR0	MR1
1	MR1	MR2
2	MR2	MR3
3	MR3	MR4
4	MR4	MR8
8	MR8	MR0

● Mode Register Write

Register Write latency is fixed to 1, Registers 0, 4 & 8 are read and writable, Registers 1, 2 and 3 are read-only, and Register 6 is write-only.

Figure 15 - Mode Register Write

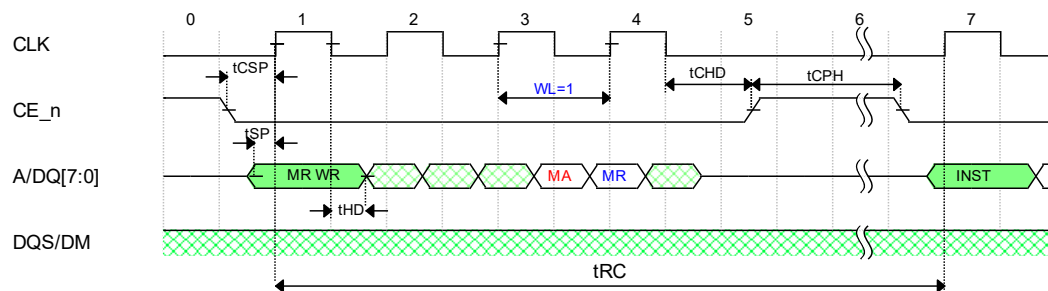


Table 15— MA decoder for MR Write

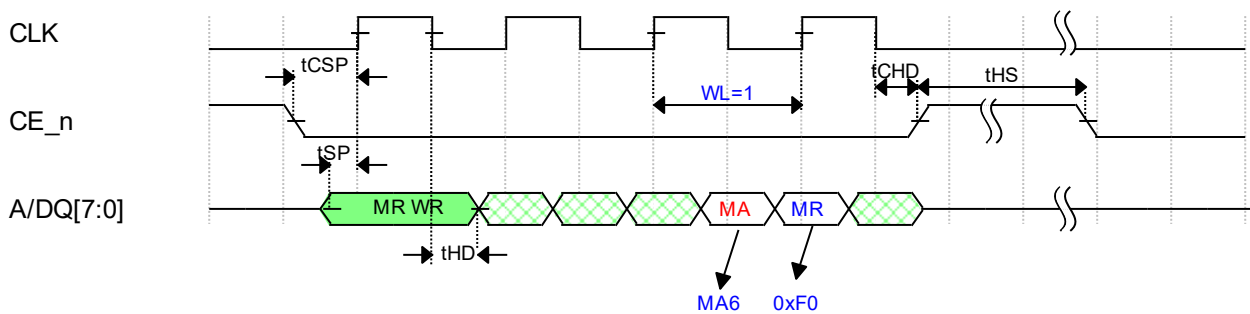
MA	MR
0	MR0
4	MR4
6	MR6
8	MR8

3 Low power features

3.1 Half Sleep Mode

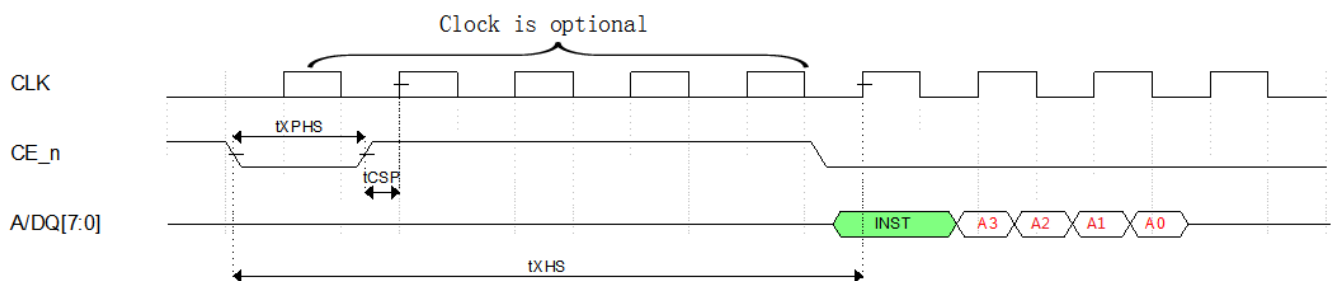
Half Sleep Mode puts the device in an ultra-low power mode with array data is retained. Half Sleep Mode is entered by writing 0xF0 into MR6. CE_n going high initiates the PSRAM into Half Sleep Mode and must be maintained for the minimum duration of t_{HS}. As shown in Figure 15

Figure 16 - Half Sleep Mode Entry



Half Sleep Exit is initiated by a low pulsed CE_n. Afterwards, CE_n can be held high with or without clock toggling until the first operation begins (observing minimum t_{XHS}).

Figure 17 - Half Sleep Mode Exit



4 Operating Conditions and Interface Specification

4.1 Absolute Maximum Ratings

Table 16 - Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Note
		Min.	Max.		
Voltage to any ball except VDD, VDDQ relative to VSS	VT	-0.4	VDD/VDDQ+0.4	V	
Voltage on VDD supply relative to VSS	VDD	-0.4	+ 2.45	V	
Voltage on VDDQ supply relative to VSS	VDDQ	-0.4	+ 2.45	V	
Storage Temperature	T _{STG}	-55	+150	°C	1)

Notes:

Storage temperature refers to the case surface temperature on the center/top side of the PSRAM.

Caution:

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

4.2 Pin Capacitance

Table 17- Bare Die Pin Capacitance

Parameter	Symbol	Min.	Max.	Unit	Note
Input Pin Capacitance	C _{IN}		1	pF	V _{IN} =0V
Output Pin Capacitance	C _{OUT}		2	pF	V _{OUT} =0V

Notes:

1) spec condition is 25°C.

Table 18- Package Pin Capacitance

Parameter	Symbol	Min.	Max.	Unit	Note
Input Pin Capacitance	C _{IN}		TBD	pF	V _{IN} =0V
Output Pin Capacitance	C _{OUT}		TBD	pF	V _{OUT} =0V

Notes:

1) spec condition is 25°C.

Table 19- Load Capacitance

Parameter	Symbol	Min.	Max.	Unit	Note
Load Capacitance	C _L		15	pF	

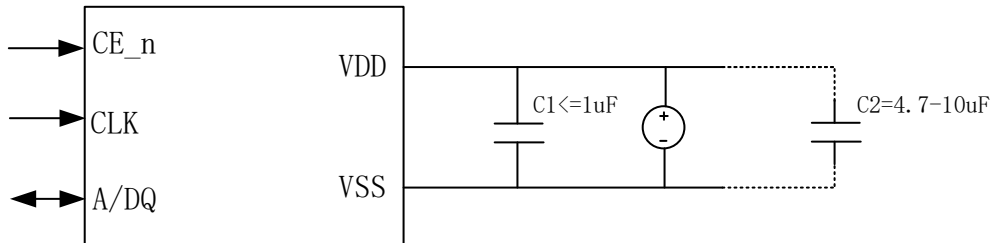
Notes:

1) System C_L for the use package.

4.3 Decoupling Capacitor Requirement

System designers need to take care of power integrity considering voltage regulator response and the memory peak currents/usage modes.

Figure 18 - Decoupling Capacitor



- Low ESR cap C1

It is recommended to place a low ESR decoupling capacitor of $\leq 1\mu\text{F}$ close to the device to absorb transient peaks.

- Large cap C2

During Half-sleep modes even though half-sleep average currents are very small (less than $100\mu\text{A}$), its peak current from internal periodical burst refresh can reach up to the level of 25mA . The peak current duration can last for few tens of microseconds. During this period if the system regulator cannot supply such large peaks, it is important to place a $4.7\mu\text{F}$ - $10\mu\text{F}$ cap to cover the burst refresh current demand and replenish the cap before the next burst of refresh.

4.4 Operating Conditions

Table 20– Operating Temperature

Parameter	Min.	Max.	Unit	Note
Operating Temperature (extended 1)	-40	125	°C	
Operating Temperature (extended 2)	-40	105	°C	
Operating Temperature (standard)	-40	85	°C	

4.5 ISB Partial Array Refresh Current

Table 21- Typical PASR Current @ 25°C

Standby Current @ 25°C			
PASR	ISB –typical mean	Unit	Notes
Full	53	μA	1),2)
1/2	45	μA	1),2)
1/4	41	μA	1),2)
1/8	39	μA	1),2)
Half Sleep Current @ 25°C			
PASR	I Half Sleep-typical mean	Unit	Notes
Full	22	μA	1),2),3)
1/2	18	μA	1),2),3)
1/4	16	μA	1),2),3)
1/8	14	μA	1),2),3)

Table 22- Typical PASR Current @ 125°C/105°C/85°C

Standby Current @ 85°C			
PASR	ISB –typical mean	Unit	Notes
Full	180	μA	2)
1/2	114	μA	2)
1/4	80	μA	2)
1/8	63	μA	2)
Half Sleep Current @ 85°C			
PASR	I Half Sleep-typical mean	Unit	Notes
Full	128	μA	2),3)
1/2	74	μA	2),3)
1/4	47	μA	2),3)
1/8	34	μA	2),3)
Standby Current @ 105°C			
PASR	ISB –typical mean	Unit	Notes
Full	320	μA	2)
1/2	201	μA	2)
1/4	135	μA	2)
1/8	101	μA	2)
Half Sleep Current @ 105°C			
PASR	I Half Sleep-typical mean	Unit	Notes
Full	261	μA	2),3)
1/2	151	μA	2),3)
1/4	97	μA	2),3)
1/8	69	μA	2),3)
Standby Current @ 125°C			
PASR	ISB –typical mean	Unit	Notes
Full	593	μA	2)
1/2	337	μA	2)
1/4	216	μA	2)
1/8	147	μA	2)
Half Sleep Current @ 125°C			
PASR	I Half Sleep-typical mean	Unit	Notes
Full	486	μA	2),3)
1/2	268	μA	2),3)
1/4	159	μA	2),3)
1/8	104	μA	2),3)

Note:

- 1) Slow Refresh current is only attainable by enabling 0.5x Refresh Frequency (see Table 17)
- 2) PASR Current is only characterized without CLK toggling.
- 3) Half Sleep current is only guaranteed after 150ms into Half Sleep mode.

4.6 DC Characteristics

Table 23- DC Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
VDD	Supply Voltage	1.62	1.98	V	
VDDQ	I/O Supply Voltage	1.62	1.98	V	
V _{IH}	Input high voltage	VDDQ-0.4	VDDQ+0.3	V	
V _{IL}	Input low voltage	-0.3	0.4	V	
V _{OH}	Output high voltage (IOH=-0.2mA)	0.8 VDDQ		V	
V _{OL}	Output low voltage (IOL=+0.2mA)		0.2 VDDQ	V	
I _{LI}	Input leakage current		1	μA	
I _{LO}	Output leakage current		1	μA	
ICC	Write @13MHz (x8/x16) (-40°C to 125°C)		5/5	mA	1)
	Write @133MHz (x8/x16) (-40°C to 125°C)		12/17	mA	1)
	Write @166MHz (x8/x16) (-40°C to 125°C)		14/20	mA	1)
	Write @200MHz (x8/x16) (-40°C to 125°C)		16/23	mA	1)
	Write @225MHz (x8/x16) (-40°C to 125°C)		17/26	mA	1)
	Write @250MHz (x8/x16) (-40°C to 125°C)		19/28	mA	1)
	Write @300MHz (x8/x16) (-40°C to 125°C)		22/33	mA	1)
	Write @333MHz (x8/x16) (-40°C to 125°C)		24/36	mA	1)
	Write @400MHz (x8/x16) (-40°C to 125°C)		27/43	mA	1)
	Read @13MHz (x8/x16) (-40°C to 125°C)		5/6	mA	1)
	Read @133MHz (x8/x16) (-40°C to 125°C)		15/23	mA	1)
	Read @166MHz (x8/x16) (-40°C to 125°C)		17/27	mA	1)
	Read @200MHz (x8/x16) (-40°C to 125°C)		20/32	mA	1)
	Read @225MHz (x8/x16) (-40°C to 125°C)		22/36	mA	1)
	Read @250MHz (x8/x16) (-40°C to 125°C)		23/39	mA	1)
	Read @300MHz (x8/x16) (-40°C to 125°C)		27/46	mA	1)
	Read @333MHz (x8/x16) (-40°C to 125°C)		30/50	mA	1)
	Read @400MHz (x8/x16) (-40°C to 125°C)		35/59	mA	1)
ISB _{EXT1}	Standby current (extended temp 1)		778	μA	2)
ISB _{EXT2}	Standby current (extended temp 2)		409	μA	2)
ISB _{STD}	Standby current (standard temp)		237	μA	2)
ISB _{STDroom}	Standby current (room temp)		68	μA	2), 3), 4)

Note:

- 1) Current is only characterized.
- 2) Without CLK toggling. ISB will be higher if CLK is toggling.
- 3) 0.5x Refresh.
- 4) Typical mean ISB_{STDROOM} 53μA.
- 5) Current is only guaranteed after 150ms into Half Sleep mode.

4.7 AC Characteristics

Table 24- READ/WRITE Timing

		BGA 1.8V Only															
		166MHz		200MHz		225MHz		250MHz		300MHz		333MHz		400MHz			
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
tCLK	CLK period	6		5		4.4		4		3.3		3		2.5		ns	
tCH/tCL	Clock high/low width	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCLK	
tKHL	CLK rise or fall time		1		0.8		0.7		0.6		TBD		TBD		TBD	ns	
tCPH	CE# HIGH between subsequent burst operations	22		24		26		28		30		32		35		ns	
tCEM	CE# low pulse width (excluding Half Sleep exit)		4		4		4		4		4		4		4	μs	Standard temp
			1		1		1		1		1		1		1	μs	Extended temp 2
			0.5		0.5		0.5		0.5		0.5		0.5		0.5	μs	Extended temp 1
tCEM	CE# low pulse width	3		3		3		3		3		3		3		tCLK	Min. 3 clocks
tCSP	CE# setup time to CLK rising edge	2		2		2		2		1.5		1.5		1.5		ns	Note1
tCHD	CE# hold time from CLK falling edge	2		2		2		2		1.5		1.5		1.5		ns	Note1
tSP	Setup time to active CLK edge	0.6		0.5		0.45		0.4		0.4		0.4		0.4		ns	
tHD	Hold time from active CLK edge	0.6		0.5		0.45		0.4		0.4		0.4		0.4		ns	Max. 0.75*tCLK
tHZ	Chip disable to DQ/DQS output high-Z		6.5		6.5		6.5		6.5		6.5		6.5		6.5	ns	
tRC	Write Cycle	60		60		60		60		60		60		60		ns	
tRC	Read Cycle	60		60		60		60		60		60		60		ns	
tHS	Minimum Half Sleep duration	150		150		150		150		150		150		150		μs	
tXHS	Half Sleep Exit CE# low to CLK setup	150		150		150		150		150		150		150		μs	
tXPHS	Half Sleep Exit CE# low pulsewidth	60		60		60		60		60		60		60		ns	
			2		2		2		2		2		2		2	μs	Standard temp
			0.5		0.5		0.5		0.5		0.5		0.5		0.5	μs	Extended temp
tPU	Device Initialization	150		150		150		150		150		150		150		μs	
tRP	RESET# low pulse width	1		1		1		1		1		1		1		μs	
tRST	Reset to CMD valid	2		2		2		2		2		2		2		μs	

Note1: It is strongly recommend to stop clock when CE_n is high;

If clock is toggling when CE_n is high, the following conditions must be satisfied:

- 1). tCSP must be satisfied;

2). If tCHD could not be satisfied, the minimal value of $tCHD = tCLK/2 - tCSPmin$ should be guaranteed;

Table 25– DDR Timing Parameters

		BGA 1.8V Only															
		166MHz		200MHz		225MHz		250MHz		300MHz		333MHz		400MHz			
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
tCQLZ	Clock rising edge to DQS low	1	7	1	7	1	7	1	7	1	7	1	7	1	7	ns	
tDQSCK	DQS output access time from CLK	2	5	2	5	2	5	2	5	2	5	2	5	2	5	ns	
tDQSQ	DQS – DQ skew		0.5		0.4		0.4		0.4		0.4		0.4		0.4	ns	
tDS	DQ and DM input setup time	0.6		0.5		0.45		0.4		0.4		0.4		0.4		ns	
tDH	DQ and DM input hold time	0.6		0.5		0.45		0.4		0.4		0.4		0.4		ns	

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