Feb. 2025

SCA16GS03C2F1C-56B

262-Pin DDR5 Unbuffered SODIMM(X64,Non-ECC)

EU RoHS Compliant

Data Sheet

Rev. A

Revision History		
Date	**Revision**	**Subjects (major changes since last revision)**
2025-02	A	Initial Release

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Contents

1 Overview

This chapter gives an overview of the 262-pin DDR5 SODIMM product family and describes its main characteristics.

1.1 Features

- 262-Pin PC5-5600 DDR5 SODIMM
- On-DIMM SPD EEPROM with hub function and integrated temperature sensor (TS)
- On-DIMM Power management integrated circuit (PMIC)
- Frequency/CAS latency: 0.357ns @ CL = 56 (DDR5-5600)
- VDD = VDDQ = 1.1V
- VPP = 1.8V
- On-die, internal, adjustable V_{REF} generation for DQ, CA, CS
- 32 internal banks: 8 groups of 4 banks each
- 16n-bit prefetch architecture
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated clock, control, command and address bus
- Anti-Sulfurated Option

Table 1 - Module Performance Table

UniIC Speed Code		**-56B**	**Unit**	**Note**
DRAM Speed Grade	**DDR5**	**-5600**		
CAS-RCD-RP latencies		**-46-45-45**	**t_{CK}**	
Min. RAS-CAS-Delay	t_{RCD}	16	ns	
Min. Row Precharge Time	t_{RP}	16	ns	
Min. Row Active Time	t_{RAS}	32	ns	
Min. Row Cycle Time	t_{RC}	48	ns	

1.2 Description

The UniIC 16GB module family are SODIMM with 30mm height based on DDR5 technology.

DIMMs intended for mounting into 262-pin connector sockets.

Table 2 - Ordering Information

Product Type	Compliance Code[1)]	Description	SDRAM Technology
PC5-5600 (46-45-45)			
SCA16GS03C2F1C-56B	16GB 1R×8 PC5-5600-46-45-45	1Rank	16Gbit (×8)

1) This describes the speed grade, for example " PC5-5600-46-45-45" where 5600 means DIMM modules with 5600MT/s data rate and "46-45-45" means Column Address Strobe (CAS) latency=46, Row Column Delay (RCD) latency = 45 and Row Precharge (RP) latency = 45.

Table 3 - Address Format

DIMM Density	**16GB(1Rx8,x64)**
Row address	64K A[15:0]
Column address	1K A[9:0]
Device bank group address	8 BG[2:0]
Device bank address per group	4 BA[1:0]
Device configuration	16Gb(2Gx8)
Device Quantity	8

2 Pin Configurations

2.1 Pin Configurations

The pin configuration of the 262-Pin SODIMM is listed by function in **Table 4** (262 pins).

Table 4 - Pin Configuration SODIMM (262 pin)

262-Pin DDR5 SODIMM Front							
Pin	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**197**	**Vss**
1	VIN_BULK	67	Vss	131	CK0_A_t	199	DQ8_B
3	VIN_BULK	69	DQ22_A	133	CK0_A_c	201	Vss
5	RFU	71	Vss	135	Vss	203	DQ10_B
7	PWR_GOOD	73	DQ24_A	137	CK0_B_t	205	Vss
9	Vss	75	Vss	139	CK0_B_c	207	DQS1_B_c
11	DQ0_A	77	DQ26_A	141	Vss	209	DQS1_B_t
13	Vss	79	Vss	143	RFU	211	Vss
15	DQ2_A	81	DQS3_A_c	145	CA11_B	213	DQ12_B
17	Vss	83	DQS3_A_t	147	Vss	215	Vss
19	DM0_A_n	85	Vss	149	CA9_B	217	DQ14_B
21	Vss	87	DQ28_A	151	CA7_B	219	Vss
23	DQ4_A	89	Vss	153	Vss	221	DQ16_B
25	Vss	91	DQ30_A	155	CA5_B	223	Vss
27	DQ6_A	93	Vss	157	CA3_B	225	DQ18_B
29	Vss	95	CB0_A	159	Vss	227	Vss
31	DQ8_A	97	Vss	161	CS0_B_n	229	DM2_B_n
33	Vss	99	CB2_A	163	RESET_n	231	Vss
35	DQ10_A	101	Vss	165	CS1_B_n	233	DQ20_B
37	Vss	103	CB3_A	167	Vss	235	Vss
39	DQS1_A_c	105	Vss	169	DQS4_B_c	237	DQ22_B
41	DQS1_A_t	107	CA0_A	171	DQS4_B_t	239	Vss
43	Vss	109	CA1_A	173	Vss	241	DQ24_B
45	DQ12_A	111	Vss	175	CB3_B	243	Vss
47	Vss	113	CA2_A	177	Vss	245	DQ26_B
49	DQ14_A	115	CA4_A	179	DQ0_B	247	Vss
51	Vss	117	Vss	181	Vss	249	DQS3_B_c
53	DQ16_A	119	CA6_A	183	DQ2_B	251	DQS3_B_t
55	Vss	121	CA8_A	185	Vss	253	Vss
57	DQ18_A	123	Vss	187	DM0_B_n	255	DQ28_B
59	Vss	125	CA10_A	189	Vss	257	Vss
61	DM2_A_n	KEY		191	DQ4_B	259	DQ30_B
63	Vss	127	CA12_A	193	Vss	261	Vss
65	DQ20_A	129	Vss	195	DQ6_B		

262-Pin DDR5 SODIMM Back							
Pin	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**198**	**DQ7_B**
2	HSA	68	DQ21_A	132	CK1_A_t	200	Vss
4	HSCL	70	Vss	134	CK1_A_c	202	DQ9_B
6	HSDA	72	DQ23_A	136	Vss	204	Vss
8	PWR_EN	74	Vss	138	CK1_B_t	206	DQ11_B
10	Vss	76	DQ25_A	140	CK1_B_c	208	Vss
12	DQ1_A	78	Vss	142	Vss	210	DM1_B_n
14	Vss	80	DQ27_A	144	CA12_B	212	Vss
16	DQ3_A	82	Vss	146	CA10_B	214	DQ13_B
18	Vss	84	DM3_A_n	148	Vss	216	Vss
20	DQS0_A_c	86	Vss	150	CA8_B	218	DQ15_B
22	DQS0_A_t	88	DQ29_A	152	CA6_B	220	Vss
24	Vss	90	Vss	154	Vss	222	DQ17_B
26	DQ5_A	92	DQ31_A	156	CA4_B	224	Vss
28	Vss	94	Vss	158	CA2_B	226	DQ19_B
30	DQ7_A	96	CB1_A	160	Vss	228	Vss
32	Vss	98	Vss	162	CA1_B	230	DQS2_B_c
34	DQ09_A	100	DQS4_A_c	164	CA0_B	232	DQS2_B_t
36	Vss	102	DQS4_A_t	166	Vss	234	Vss
38	DQ11_A	104	Vss	168	CB0_B	236	DQ21_B
40	Vss	106	CS0_A_n	170	Vss	238	Vss
42	DM1_A_n	108	ALERT_n	172	CB1_B	240	DQ23_B
44	Vss	110	CS1_A_n	174	Vss	242	Vss
46	DQ13_A	112	Vss	176	CB2_B	244	DQ25_B
48	Vss	114	CA3_A	178	Vss	246	Vss
50	DQ15_A	116	CA5_A	180	DQ1_B	248	DQ27_B
52	Vss	118	Vss	182	Vss	250	Vss
54	DQ17_A	120	CA7_A	184	DQ3_B	252	DM3_B_n
56	Vss	122	CA9_A	186	Vss	254	Vss
58	DQ19_A	124	Vss	188	DQS0_B_c	256	DQ29_B
60	Vss	126	CA11_A	190	DQS0_B_t	258	Vss
62	DQS2_A_c	KEY		192	Vss	260	DQ31_B
64	DQS2_A_t	128	RFU	194	DQ5_B	262	Vss
66	Vss	130	Vss	196	Vss		

2.2 Pin Descriptions

Table 5 - Pin Descriptions

Symbol	Type	I/O Level	Description
CK[1:0]_A_t CK[1:0]_B_t CK[1:0]_A_c CK[1:0]_B_c	Input	VDDQ	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA[12:]0_A CA[12:]0_B	Input	VDDQ	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi-cycle, the pins may not be interchanged between devices on the same bus. The address inputs also provide the op-code during MODE REGISTER SET commands.
CS[1:0]_A_n CS[1:0]_B_n	Input	VDDQ	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external rank selection on systems with multiple ranks. CS_n is considered part of the command code. CS_n is also used to enter and exit the parts from power down mode and self refresh mode. While not in self refresh mode the CS_n input buffer operates with the same ODT and V_{REF} parameters as configured by the CA_ODT strap setting or mode register. When in self refresh, the CS_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of VDD.
ALERT_n	Output	VDDQ	Alert: If there is an error in CRC, then ALERT_n drives LOW for the period time interval and returns HIGH. During connectivity test mode, this pin functions as an input. Usage of this signal is system-dependent. In the case where this pin is not connected, ALERT_n must be bonded to V_{DDQ} on the system board.
RESET_n	Input	VDDQ	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of VDDQ.
Power_Good	Input/Output	VDDQ	Power Good Indicator: Open drain output. The PMIC ensures this pin HIGH when VIN_Bulk input supply, as well as all enabled output buck regulators and all LDO regulators tolerance threshold is maintained as configured in the appropriate register. The PMIC drives this pin LOW when VIN_Bulk input goes below the threshold or when any of the enabled output buck regulator exceeds the thresholds configured in the appropriate register or when any LDO output regulator exceeds the threshold configured in the appropriate register. As an input, the PMIC disables its output regulator when this pin is LOW. The LDO outputs remain on.
HSCL	Input	VOUT_1.0V	Host Sideband Bus Clock: Bus clock used to strobe data into HUB device. When open drain, a pull-up resistor is required on the system motherboard.
HSDA	Input/Output	VOUT_1.0V	Host Sideband Bus Data: I2C/I3C-Basic data. When open drain, a pull-up resistor is required on the system motherboard.
HSA	Input	GND	Host Sideband Bus Device ID: Address input to a hub or other client device to distinguish between identical devices in the I3C basic address range. Tied to GND, HSA has different resistor values on the motherboard to identify DIMM slot address. Refer to the SPD Hub spec for more information.

Symbol	Type	I/O Level	Description
DQ[31:0]_A DQ[31:0]_B	Input/Output	VDDQ	Data Input/Output: Bidirectional data bus. If CRC is enabled via the mode register, then CRC code is added at the end of data burst. Any DQ from DQ0—DQ3 may indicate the internal V_{REF} level during test via mode register setting MR4 A4 = HIGH. Refer to the vendor-specific data sheets to determine which DQ is used.
CB[7:0]_A CB[7:0]_B	Input/Output	VDDQ	ECC Check Bits Input/Output: Bidirectional data bus on UDIMM With ECC
DQS[4:0]_A_t DQS[4:0]_B_t DQS[4:0]_A_c DQS[4:0]_B_c	Input/Output	VDDQ	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR5 SDRAM only supports differential data strobe. It does not support single-ended strobe.
DM[3:0]_A_n DM[3:0]_B_n	Input	VDDQ	Input Data Mask: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. For x8 device, the function of DM_n is enabled by MR5:OP[5] = 1.
PWR_EN	Input	3.3V	PMIC Enable. When this pin is high, the PMIC turns on the regulator. When this pin is low, the PMIC turns off the regulator. This signal is connected to PMIC's VR_EN pin.
VIN_BULK	Supply		External Power Supply: 5V, 4.25V (min), 5.5V (max)
VSS	Supply		Ground
RFU			Reserved for future use. No on DIMM electrical connection is present.
NC			No connect: No internal electrical connection is present.
NF			No function: May have internal connection present, but has no function.

3 General Description

3.1 General Description

High-speed DDR5 SDRAM modules use DDR5 SDRAM devices with four or eight internal memory bank groups. DDR5 SDRAM modules benefit from DDR5 SDRAM's use of a 16n-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single READ or WRITE operation for the DDR5 SDRAM effectively consists of a single 16n-bit-wide, eight-clock data transfer at the internal DRAM core and sixteen corresponding n-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR5 modules use two sets of differential signals (DQS_t and DQS_c) to capture data, and CK_t and CK_c to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

3.2 Power Management Integrated Circuit Operation

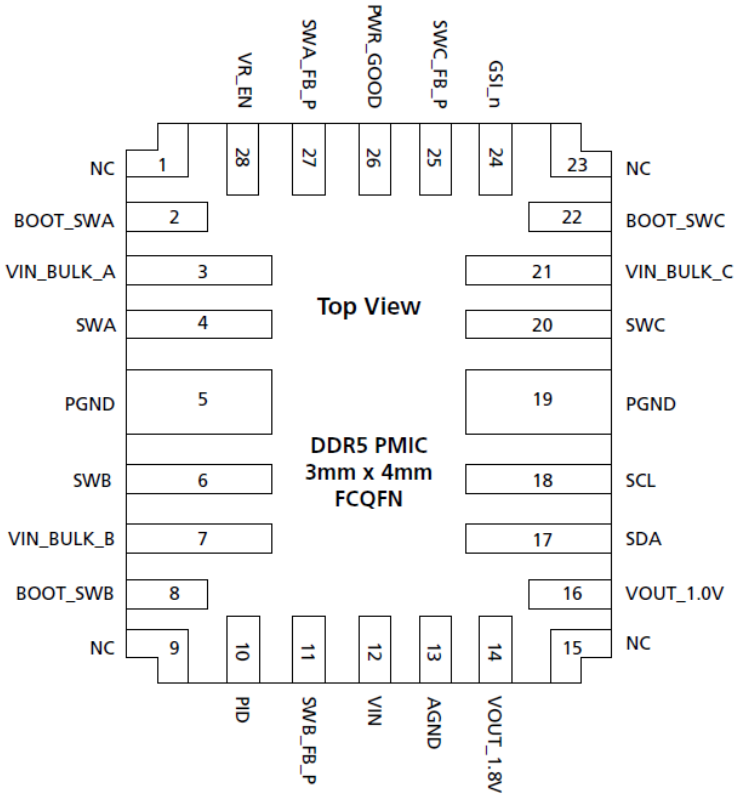
The power management integrated circuit (PMIC) is new for DDR5. For SODIMMs, JEDEC defines PMIC5100. This operation converts a 5V supply into regulated values for components on the module. The PMIC allows the host to monitor voltage and current via the sideband channel.

The PMIC5100 has one 5V nominal supply input pin from the card edge through VIN_Bulk. The PMIC has the ability to regulate lower voltages to the HUB which allows external access to read/configure this device prior to the VR ENABLE command. The VIN_Bulk supply, after the VR ENABLE command, will supply all regulated voltages to the PMIC and DRAM.

By default, the PMIC powers up in I2C mode, and the host can reconfigure to support I3C-basic if needed. Please see the address configuration as below table for the PMIC Address ID (PID), device pin #10.

Table 6 - PMIC Addressing

PID Configuration (Pin #10)	PMIC Address ID (PID)			
	Bit 7	Bit 6	Bit 5	Bit 4
Pin to Vss	1	0	0	1



3.3 SPD EEPROM HUB Operation

DDR5 SDRAM modules incorporate an SPD EEPROM with hub function with integrated thermal sensor (TS). The SPD data is stored in a 1024-byte including16 blocks (64 bytes per block), and each block may optionally be write-protected via software command.

The EEPROM resides on a two-wire I3C serial interface, which is also compatible with legacy I2C interface and is not integrated with the memory bus in any manner. It operates as an initiator/target device in the I3C-basic protocol, with all operations synchronized by the serial clock. Transfer rates of up to 12.5 MHz are achievable at 1.0V (NOM).

The first 640 bytes are programmed by UniIC for DIMM parameters related usage. The remaining 384 bytes are available for the end user.

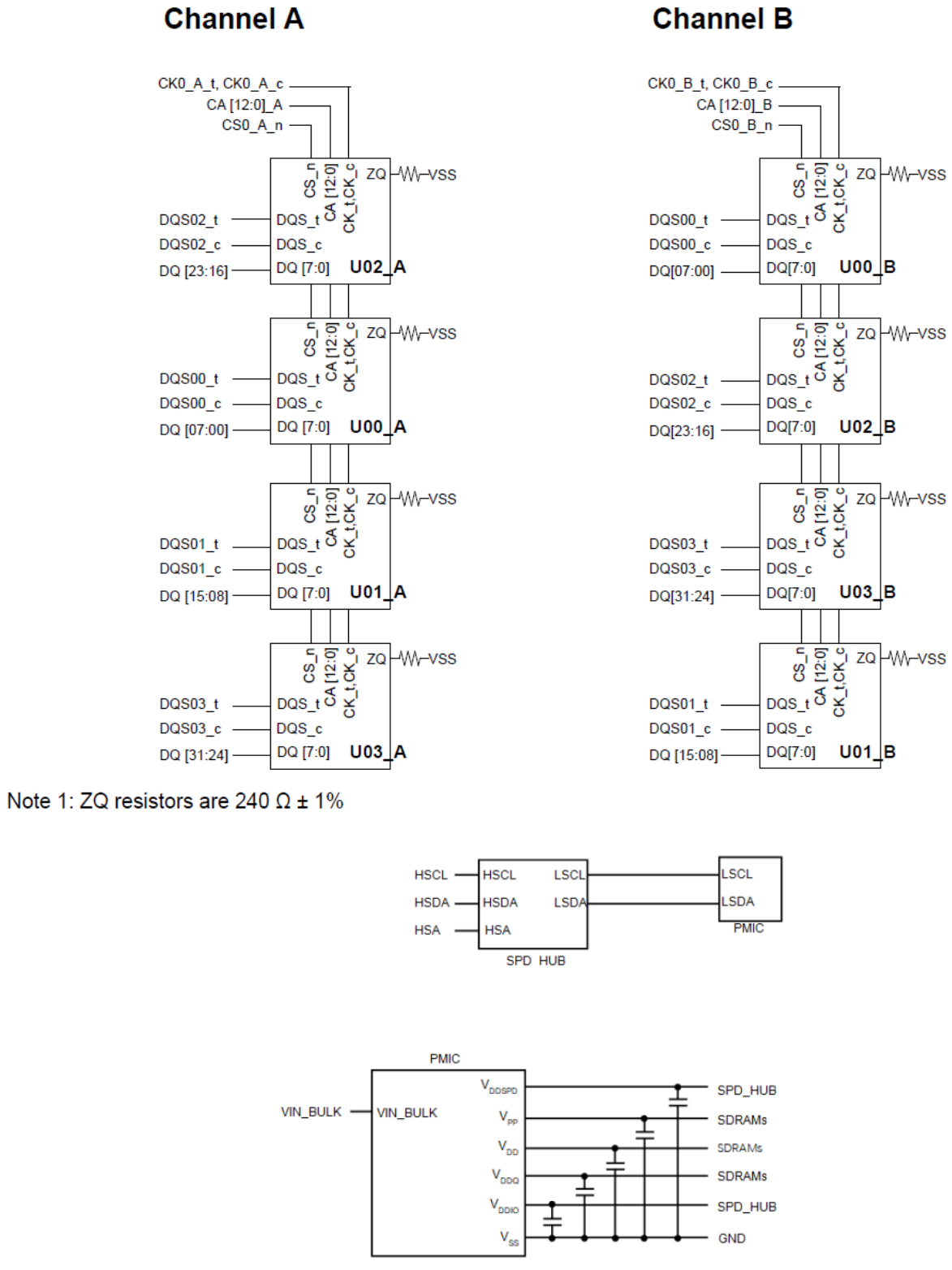
UniIC implements reversible software write protection on DDR5 SDRAM-based modules. This prevents the lower 640 bytes (bytes 0 to 639) from being inadvertently programmed or corrupted. The upper 384 bytes remain available for customer use and are unprotected.

Table 7 - SPD Byte Information

Block	Range		Description
0	0~63	0x000~0x03F	Base configuration and DRAM parameters
1	64~127	0x040~0x07F	Base configuration and DRAM parameters
2	128~191	0x080~0x0BF	Reserved for future use
3	192~239	0x0C0~0x0EF	Common Module Parameters -- See annex A.0 for details
	240~255	0x0D0~0x0FF	Standard module parameters -- See annexes A.x for details
4	256~319	0x100~0x13F	Standard module parameters -- See annexes A.x for details
5	320~383	0x140~0x17F	Standard module parameters -- See annexes A.x for details
6	384~447	0x180~0x1BF	Standard module parameters -- See annexes A.x for details
7	448~509	0x1C0~0x1FF	Reserved for future use
	510~511	0x1FE~0x1FF	CRC for SPD bytes 0~509
8	512~575	0x200~0x23F	Manufacturing information
9	576~639	0x240~0x27F	Manufacturing information
10	640~703	0x280~0x2BF	End user programmable
11	704~767	0x2C0~0x2FF	End user programmable
12	768~831	0x300~0x33F	End user programmable
13	832~895	0x340~0x37F	End user programmable
14	896~959	0x380~0x3BF	End user programmable
15	960~1023	0x3C0~0x3FF	End user programmable

3.4 Function Block Diagram

Figure 1 - Function Block Diagram_SCA16GS03C2F1C-56B



3.5 DQ Map

Table 8 - DQ Map _SCA16GS03C2F1C-56B

Module Pin NO.	Module DQ NO.	IC NO.	IC DQ	Module Pin NO.	Module DQ NO.	IC NO.	IC DQ
11	0_A	U00_A	0	31	8_A	U01_A	1
12	1_A		1	34	9_A		0
15	2_A		2	35	10_A		3
16	3_A		3	38	11_A		2
23	4_A		6	45	12_A		5
26	5_A		5	46	13_A		6
27	6_A		4	49	14_A		7
30	7_A		7	50	15_A		4
53	16_A	U02_A	0	73	24_A	U03_A	1
54	17_A		1	76	25_A		0
57	18_A		2	77	26_A		3
58	19_A		3	80	27_A		2
65	20_A		6	87	28_A		5
68	21_A		5	88	29_A		6
69	22_A		4	91	30_A		7
72	23_A		7	92	31_A		4
179	0_B	U00_B	0	199	8_B	U01_B	1
180	1_B		1	202	9_B		0
183	2_B		2	203	10_B		3
184	3_B		3	206	11_B		2
191	4_B		6	213	12_B		5
194	5_B		5	214	13_B		6
195	6_B		4	217	14_B		7
198	7_B		7	218	15_B		4
221	16_B	U02_B	0	241	24_B	U03_B	1
222	17_B		1	244	25_B		0
225	18_B		2	245	26_B		3
226	19_B		3	248	27_B		2
233	20_B		6	255	28_B		5
236	21_B		5	256	29_B		4
237	22_B		4	259	30_B		7
240	23_B		7	260	31_B		6

4 Electrical Characteristics

4.1 AC and DC Operation Conditions

Table 9 - Absolute Maximum DC Ratings

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-0.3	+1.4	V	1)
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	-0.3	+1.4	V	1)
V_{PP}	Voltage on V_{PP} pin relative to V_{SS}	-0.3	+2.1	V	3)
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.3	+1.4	V	1)
T_{STG}	Storage Temperature	-55	+100	°C	1),2)

Notes:

1) Stresses greater than those listed in this table may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2) Storage temperature is the case surface temperature on the center/top side of the device. For the measurement conditions, refer to JESD51-2 standard.

3) VPP must be equal or greater than VDD /VDDQ at all times during power on and operation of DRAM device.

Table 10 - DC Voltage Operating Conditions

Symbol	Parameter	Low Frequency Voltage Spec			Unit	Note
		Min.	Typ	Max.		
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	1.067(-3%)	1.1	1.166(+6%)	V	1), 2)
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	1.067(-3%)	1.1	1.166(+6%)	V	1), 2)
V_{PP}	Voltage on V_{PP} pin relative to V_{SS}	1.746(-3%)	1.8	1.908(+6%)	V	1), 2)

Notes:

1) VDD must be within 66mV of VDDQ.

2) AC parameters are measured with VDD and VDDQ tied together.

Table 11 - DRAM Component Operating Temperature Range

Symbol	Parameter	Rating		Unit	Grade	Note
		Min.	Max.			
T_{OPER_NORMAL}	Normal Operating Temperature	0	85	°C	NT	1),2),3),4)
$T_{OPER\_EXTENDED}$	Extended Operating Temperature	0	95	°C	XT	1),2),3),4)

Notes:

1) All operating temperature symbols, ranges, acronyms from JESD402-1.
2) Operating Temperature is the case surface temperature on the center / top side of the DRAM. For the measurement conditions, refer to JESD51-2.
3) All devices are required to operate in NT and XT temperature ranges.
4) When operating above 85°C, the host shall provide appropriate refresh mode controls associated with increased temperature range. The full description of these settings are defined in the tREFI parameters for REFab and REFsb command by device density table in the Refresh operations section (DRAM datasheet).

4.2 Module and Component Speed Grades

DDR5 components may exceed the listed module speed grades; module may not be available in all listed speed grades

Table 12 - Module and Component Speed Grades

Module Speed Grade	Component Speed Grade
-56B	5600-46-45-45

4.3 I_{DD} Specifications

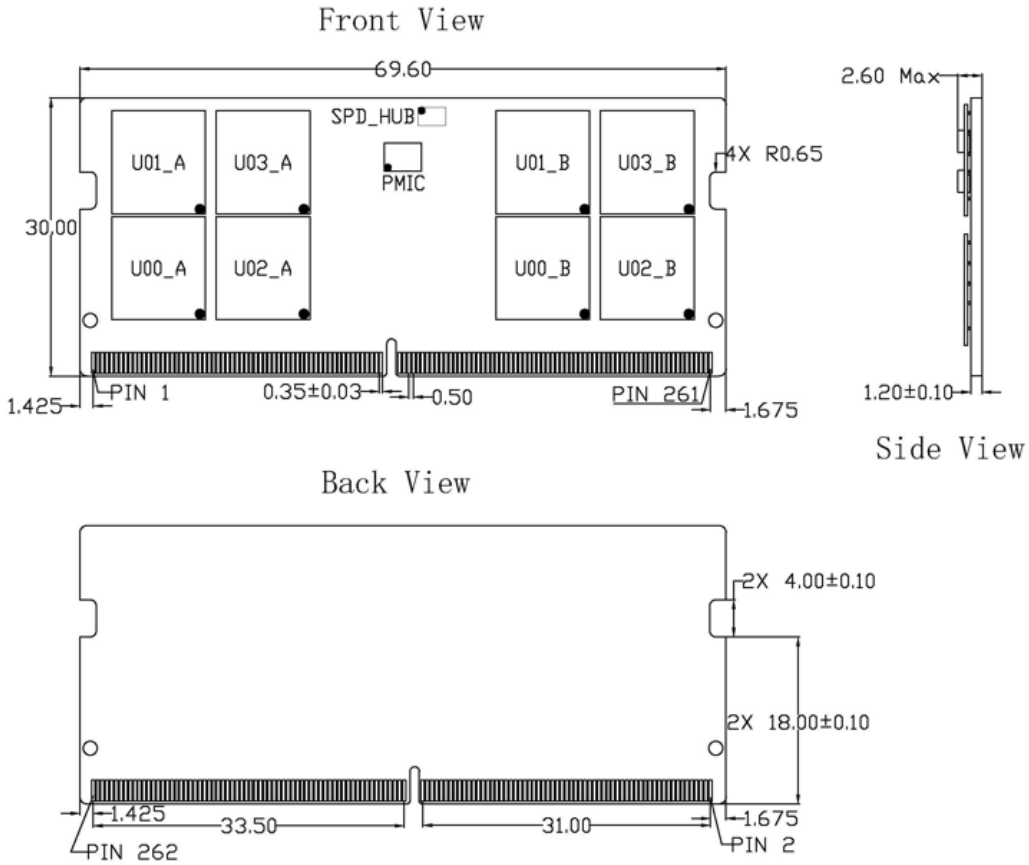
Table 13 - I_{DD} Specification for SCA16GS03C2F1C-56B

Module IDD is based on PMIC VIN_BULK 5V input current and typical operating temperature. Each IDD parameter includes PMIC efficiency and all DRAM current on all supplies (VDD, VDDQ and VPP).

Product Type		SCA16GS03C2F1C-56B	Unit	Note
Organization		16GB		
		1Rank (×8)		
		×64		
		-56B		
Parameter	Symbol	Current		
Operating one bank ACTIVATE-PRECHARGE current	IDD0	181	mA	
Operating four bank ACTIVATE-PRECHARGE current	IDD0F	270	mA	
Precharge standby current	IDD2N	148	mA	
Precharge power-down current	IDD2P	68	mA	
Active standby current	IDD3N	232	mA	
Active power-down current	IDD3P	72	mA	
Operating burst read current	IDD4R	635	mA	
Operating burst write current	IDD4W	589	mA	
Burst refresh (normal refresh mode) current	IDD5B	562	mA	
Burst refresh (fine granularity refresh mode) current	IDD5F	529	mA	
Burst refresh (same bank refresh mode) current	IDD5C	281	mA	
Self refresh current	IDD6N	43	mA	
Operating bank interleave read current	IDD7	911	mA	
Maximum power saving deep power down mode current	IDD8	16	mA	

5 Package Dimensions

Figure 2 - Package Dimensions_SCA16GS03C2F1C-56B



Note: 1. All dimensions are in millimeters.
2. The dimensional diagram is for reference only.

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Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest UniIC Office.
UniIC Components may only be used in life-support devices or systems with the express written approval of UniIC, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

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