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SCB12Q4Gxx0AF

4Gbit DDR4 SDRAM

EU RoHS Compliant Products

Data Sheet

Rev. E

Revision History		
Date	Revision	Subjects (major changes since last revision)
2019-08	A	Initial Release
2019-10	B	Modify some type Update Product list: Add SCB12Q4G800AF-08T, SCB12Q4G160AF-08T
2020-05	C	Update package outline of x 16 Product: Modify some typo. Format review (2020-05-28)
2020-07	D	Add Table 2: 4Gbit DDR4 Addressing
2021-04	E	1. Modify Table 5: IDD & IDDQ Specification a. Update IDD values b. Add I_{DDQ4R} & I_{DDQ4W} 2. Modify Table 7 IDD6 Specification: Update IDD values

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1 Features

The 4Gbit DDR4 SDRAM offers the following key features:

- Power supply
 - VDD = VDDQ = 1.2V $\pm$ 5%
 - VPP = 2.5V – 5% + 10%
- Data rate
 - 2666Mbps (DDR4-2666)
 - 2400Mbps (DDR4-2400)
- Package
 - 78-ball FBGA
 - 96-ball FBGA
 - Lead-free
- 16 or 8 internal banks
 - 4 groups of 4 banks each (x4 and x8)
 - 2 groups of 4 banks each (x16)
- Differential clock inputs operation (CK_t and CK_c)
- Bi-directional differential data strobe (DQS_t and DQS_c)
- Termination Data Strobe is supported (x8 only) (TDQS_t and TDQS_c)
- Asynchronous reset is supported (RESET_n)
- ZQ calibration for Output driver by compare to external reference resistance (RZQ 240 ohm $\pm$ 1%)
- Nominal, park and dynamic On-die Termination (ODT)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge
- CAS Latency (CL): 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22 and 23 supported
- Additive Latency (AL) 0, CL-1, and CL-2 supported
- Burst Length (BL): 8 and 4 with on the fly supported
- CAS Write Latency (CWL): 9, 10, 11, 12, 14, 16 and 18 supported
- Operating case temperature range TC = 0°C to +95°C
- Refresh cycles
 - Average refresh period 7.8 μ s at 0°C TC +85°C
 - 3.9 μ s at +85°C < TC +95°C
- Fine granularity refresh is supported
- Adjustable internal generation VREFDQ
- Pseudo Open Drain (POD) interface for data input/output
- Driver strength selected by MRS
- The high-speed data transfer by the 8 bits pre-fetch
- Temperature Controlled Refresh (TCR) mode is supported
- Low Power Auto Self Refresh (LPASR) mode is supported
- Self refresh abort is supported
- Programmable preamble is supported
- Write leveling is supported
- Command/Address latency (CAL) is supported
- Multipurpose register READ and WRITE capability
- Command Address Parity (CA Parity) for command address signal error detect and inform it to controller
- Write Cyclic Redundancy Code (CRC) for DQ error detect and inform it to controller during high-speed operation
- Data Bus Inversion (DBI) for Improve the power consumption and signal integrity of the memory interface
- Data mask (DM) for write data
- Per DRAM Addressability (PDA) for each DRAM can be set a different mode register value individually and has individual adjustment
- Gear down mode (1/2 and 1/4 rate) is supported
- PPR and sPPR is supported
- Connectivity test (x16 only)
- Maximum power down mode for the lowest power consumption with no internal refresh activity
- JEDEC JESD-79-4 compliant

2 Product List

Table 1 shows all possible products within the 4Gbit DDR4 SDRAM component generation.

Table 1 - Ordering Information for 4Gbit DDR4 Component

UnilC Part Number	Max. Clock frequency	CAS-RCD-RP latencies	Speed Sort Name	Package
4Gbit DDR4 SDRAM Components in × 8 Organization (512 M × 8)				
SCB12Q4G800AF-07Q	1333 MHz	19-19-19	DDR4-2666V	PG-FBGA-78
SCB12Q4G800AF-08T	1200 MHz	17-17-17	DDR4-2400T	PG-FBGA-78
4Gbit DDR4 SDRAM Components in × 16 Organization (256 M × 16)				
SCB12Q4G160AF-07Q	1333 MHz	19-19-19	DDR4-2666V	PG-FBGA-96
SCB12Q4G160AF-08T	1200 MHz	17-17-17	DDR4-2400T	PG-FBGA-96

Table 2 - 4Gbit DDR4 Addressing

Parameter	512Mb × 8	256Mb × 16	Note
Number of bank groups	4	2	
Bank group address	BG[1:0]	BG0	
Bank count per group	4	4	
Bank address in bank group	BA[1:0]	BA[1:0]	
Row Address	32K (A[14:0])	32K (A[14:0])	
Column Address	1K(A[9:0])	1K(A[9:0])	
Page Size	1KB	2KB	

3 Ball configuration

Figure 1 - Ball out for 512Mb x8 Components (78-ball FBGA)

	1	2	3	7	8	9
A	○ VDD	○ VSSQ	○ TDQS_c	○ DM_n, DBI_n TDQS_t	○ VSSQ	○ VSS
B	○ VPP	○ VDDQ	○ DQS_c	○ DQ1	○ VDDQ	○ ZQ
C	○ VDDQ	○ DQ0	○ DQS_t	○ VDD	○ VSS	○ VDDQ
D	○ VSSQ	○ DQ4	○ DQ2	○ DQ3	○ DQ5	○ VSSQ
E	○ VSS	○ VDDQ	○ DQ6	○ DQ7	○ VDDQ	○ VSS
F	○ VDD	○ NC	○ ODT	○ CK_t	○ CK_c	○ VDD
G	○ VSS	○ NC	○ CKE	○ CS_n	○ NC	○ NC
H	○ VDD	○ WE_n/A14	○ ACT_n	○ CAS_n/A15	○ RAS_n/A16	○ VSS
J	○ VREFCA	○ BG0	○ A10/AP	○ A12/BC_n	○ BG1	○ VDD
K	○ VSS	○ BA0	○ A4	○ A3	○ BA1	○ VSS
L	○ RESET_n	○ A6	○ A0	○ A1	○ A5	○ ALERT_n
M	○ VDD	○ A8	○ A2	○ A9	○ A7	○ VPP
N	○ VSS	○ A11	○ PAR	○ NC	○ A13	○ VDD

Figure 2 - Ball out for 256Mb x16 Components (96-ball FBGA)

A	1 ○ VDDQ	2 ○ VSSQ	3 ○ DQU0	7 ○ DQSU_c	8 ○ VSSQ	9 ○ VDDQ
B	○ VPP	○ VSS	○ VDD	○ DQSU_t	○ DQU1	○ VDD
C	○ VDDQ	○ DQU4	○ DQU2	○ DQU3	○ DQU5	○ VSSQ
D	○ VDD	○ VSSQ	○ DQU6	○ DQU7	○ VSSQ	○ VDDQ
E	○ VSS	○ DMU_n/DBIU_n	○ VSSQ	○ DML_n/DBIL_n	○ VSSQ	○ VSS
F	○ VSSQ	○ VDDQ	○ DQSL_c	○ DQL1	○ VDDQ	○ ZQ
G	○ VDDQ	○ DQL0	○ DQSL_t	○ VDD	○ VSS	○ VDDQ
H	○ VSSQ	○ DQL4	○ DQL2	○ DQL3	○ DQL5	○ VSSQ
J	○ VDD	○ VDDQ	○ DQL6	○ DQL7	○ VDDQ	○ VDD
K	○ VSS	○ CKE	○ ODT	○ CK_t	○ CK_c	○ VSS
L	○ VDD	○ WE_n/A14	○ ACT_n	○ CS_n	○ RAS_n/A16	○ VDD
M	○ VREFCA	○ BG0	○ A10/AP	○ A12/BC_n	○ CAS_n/A15	○ VSS
N	○ VSS	○ BA0	○ A4	○ A3	○ BA1	○ TEN
P	○ RESET_n	○ A6	○ A0	○ A1	○ A5	○ ALERT_n
R	○ VDD	○ A8	○ A2	○ A9	○ A7	○ VPP
T	○ VSS	○ A11	○ PAR	○ NC	○ A13	○ VDD

4 Ball Description

Table 3 - Input / Output Signal Functional Description for 512Mb x8 Components (78-ball FBGA)

Ball Name	Function	Note
A0 to A14	Address inputs A10/AP: Auto precharge A12/BC_n: Burst chop	2
BA0, BA1	Bank select	2
BG0, BG1	Bank group input	2
DQ0 to DQ7	Data input/output	
DQS_t, DQS_c	Differential data strobe	
TDQS_t, TDQS_c	Termination data strobe	
CS_n	Chip select	2
RAS_n/A16 CAS_n/A15 WE_n/A14	Command input	2
ACT_n	Activation command input	2
CKE	Clock enable	2
CK_t, CK_c	Differential clock input	
DM_n	Write data mask	
DBI_n	Data bus inversion	
ODT	ODT control	2
RESET_n	Active low asynchronous reset	2
PAR	Command and address parity	
ALERT_n	Alert	
VDD	Supply voltage for internal circuit	
VSS	Ground for internal circuit	
VDDQ	Supply voltage for DQ circuit	
VSSQ	Ground for DQ circuit	
VREFCA	Reference voltage for CA	
ZQ	Reference pin for ZQ calibration	
NC	No connection	1

Note:

1. Not internally connected with die.
2. Input only pins (address, command, CKE, ODT and RESET_n) do not supply termination.

Table 4 - Input / Output Signal Functional Description for 256Mb ×16 Components (96-ball FBGA)

Ball Name	Function	Note
A0 to A14	Address inputs A10/AP: Auto precharge A12/BC_n: Burst chop	2
BA0, BA1	Bank select	2
BG0	Bank group input	2
DQU0 to DQU7 DQL0 to DQL7	Data input/output	
DQSU, DQSU_n DQSL, DQSL_n	Differential data strobe	
CS_n	Chip select	2
RAS_n/A16 CAS_n/A15 WE_n/A14	Command input	2
ACT_n	Activation command input	2
CKE	Clock enable	2
CK_t, CK_c	Differential clock input	
DMU_n, DML_n	Write data mask	
DBIU_n, DBIL_n	Data bus inversion	
ODT	ODT control	2
RESET_n	Active low asynchronous reset	2
PAR	Command and address parity	
ALERT_n	Alert	
TEN	Connectivity test mode enable	
VDD	Supply voltage for internal circuit	
VSS	Ground for internal circuit	
VDDQ	Supply voltage for DQ circuit	
VSSQ	Ground for DQ circuit	
VREFCA	Reference voltage for CA	
ZQ	Reference pin for ZQ calibration	
NC	No connection	1

Note:

1. Not internally connected with die.
2. Input only pins (address, command, CKE, ODT and RESET_n) do not supply termination.

5 Electrical Specifications

Table 5 - IDD & IDDQ Specification

Symbol	DDR4-2400		DDR4-2666		Unit
	x8	x16	x8	x16	
I_{DD0}	98	113	105	116	mA
I_{DD0A}	98	113	105	116	mA
I_{DD1}	115	143	125	158	mA
I_{DD1A}	120	147	128	160	mA
I_{DD2N}	86	90	90	93	mA
I_{DD2NA}	86	90	90	93	mA
I_{DD2NT}	90	130	96	135	mA
I_{DD2NL}	75	83	80	85	mA
I_{DD2NG}	82	85	88	90	mA
I_{DD2ND}	65	67	68	70	mA
I_{DD2N_par}	94	102	100	106	mA
I_{DD2P}	58	60	62	65	mA
I_{DD2Q}	85	90	90	95	mA
I_{DD3N}	103	110	108	115	mA
I_{DD3NA}	103	110	108	115	mA
I_{DD3P}	84	90	88	95	mA
I_{DD4R}	167	232	182	245	mA
I_{DD4RA}	172	242	187	265	mA
I_{DD4RB}	170	222	185	235	mA
I_{DDQ4R}	27	51	32	60	mA
I_{DD4W}	187	268	202	290	mA
I_{DD4WA}	189	270	217	319	mA
I_{DD4WB}	187	251	201	275	mA
I_{DD4WC}	182	258	197	280	mA
I_{DD4W_par}	185	260	198	280	mA
I_{DDQ4W}	61	122	61	122	mA
I_{DD5B}	190	195	195	200	mA
I_{DD5F2}	200	210	200	220	mA
I_{DD5F4}	165	170	175	180	mA
I_{DD7}	225	285	235	345	mA
I_{DD8}	35	35	35	35	mA

Table 6 - IPP Specification

Symbol	DDR4-2400		DDR4-2666		Unit
	X8	X16	X8	X16	
IPP0	4	8	5	9	mA
IPP1	4	8	5	9	mA
IPP2N	3	6	4	7	mA
IPP2P	3	6	4	7	mA
IPP3N	3	6	4	7	mA
IPP3P	3	6	4	7	mA
IPP4R	3	6	4	7	mA
IPP4W	3	6	4	7	mA
IPP5B	22	24	25	27	mA
IPP5F2	23	25	27	29	mA
IPP5F4	17	18	20	20	mA
IPP7	22	33	29	40	mA
IPP8	2	2	3	3	mA

Table 7 - IDD6 Specification

Symbol	Temperature Range	DDR4-2400		DDR4-2666		Unit	Notes
		IDD(max)	IPP(max)	IDD(max)	IPP(max)		
IDD6N	0 - 85 °C	40	6	40	6	mA	1
IDD6E	0 - 95 °C	45	8	45	8	mA	2
IDD6R	0 - 45 °C	35	4	35	4	mA	3
IDD6A	0 - 85 °C	40	6	40	6	mA	4

Note:

1. Applicable for MR2 settings A6 = 0 and A7 = 0.
2. Applicable for MR2 settings A6 = 0 and A7 = 1. IDD6E is only specified for devices which support the extended temperature range feature.
3. Applicable for MR2 settings A6 = 1 and A7 = 0. IDD6R is only specified for devices which support the reduced temperature range feature.
4. Applicable for MR2 settings A6 = 1 and A7 = 1. IDD6A is only specified for devices which support the auto self-refresh feature.

6 Speed Bin

Table 8 - DDR4-2400 Speed Bins

Speed Bin			DDR4-2400R		DDR4-2400T		Unit	NOTE	
CL-nRCD-nRP			16-16-16		17-17-17				
Parameter		Symbol	min	max	min	max			
Internal read command to first data		tAA	13.32	18.00	14.16 ¹⁴ (13.75) ^{5,12}	18.00	ns	12	
Internal read command to first data with read DBI enabled		tAA_DBI	tAA(min) + 3nCK	tAA(max) +3nCK	tAA(min) +3nCK	tAA(max) +3nCK	ns	12	
ACT to internal read or write delay time		tRCD	13.32		14.16 (13.75) ^{5,12}	-	ns	12	
PRE command period		tRP	13.32		14.16 (13.75) ^{5,12}	-	ns	12	
ACT to PRE command period		tRAS	32	9 x tREFI	32	9 x tREFI	ns	12	
ACT to ACT or REF command period		tRC	45.32		46.16 (45.75) ^{5,12}	-	ns	12	
	Nor	Read DBI							
CWL = 9	CL = 9	CL = 11 (Optional) ⁵	tCK(AVG)	1.5 (Optional) ^{5,12}	1.6	Reserved		ns	1,2,3,4,11
	CL = 10	CL = 12	tCK(AVG)	Reserv ed		1.5	1.6	ns	1,2,3,4,11
	CL = 10	CL = 12	tCK(AVG)	Reserv ed		Reserved		ns	4
CWL = 9,11	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	1.25	<1.5	ns	1,2,3,4,8
	CL =	CL = 14	tCK(AVG)	1.25	<1.5	(Optional) ^{5,12}		ns	1,2,3,8
	CL =	CL = 14	tCK(AVG)	1.25	<1.5	1.25	<1.5	ns	1,2,3,8
CWL = 10,12	CL =	CL = 14	tCK(AVG)	Reserv ed		Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	1.071	<1.25	ns	1,2,3,4,8
	CL =	CL = 16	tCK(AVG)	1.071	<1.25	1.071	<1.25	ns	1,2,3,8
CWL = 11,14	CL =	CL = 17	tCK(AVG)	Reserv ed		Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	0.938	<1.071	ns	1,2,3,4,8
	CL =	CL = 19	tCK(AVG)	0.937	<1.071	0.938	<1.071	ns	1,2,3,8
CWL = 12,16	CL =	CL = 18	tCK(AVG)	Reserv ed		Reserved		ns	1,2,3,4
	CL =	CL = 19	tCK(AVG)	0.833	<0.937	Reserved		ns	1,2,3,4
	CL =	CL = 20	tCK(AVG)	0.833	<0.937	0.833	<0.938	ns	
	CL =	CL = 21	tCK(AVG)	0.833	<0.937	0.833	<0.938	ns	1,2,3
Supported CL Settings			(9), 11,12,13,14,15,16,17,18		10,11,12,13,14,15,16,17,18		nCK	13	
Supported CL Settings with read DBI			(11),13,14,15,16,18,19,20,21		12,13,14,15,16,18,19,20,21		nCK		
Supported CWL Settings			9,10,11,12,14,16		9,10,11,12,14,16		nCK		

Table 9 - DDR4-2666 Speed Bins

Speed Bin				DDR4-2666V		Unit	NOTE
CL-nRCD-nRP				19-19-19			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	14.25 ¹⁴ (13.75) ^{5,12}	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(max) +3nCK	ns	12
ACT to internal read or write delay time			tRCD	14.25 (13.75) ^{5,12}	-	ns	12
PRE command period			tRP	14.25 (13.75) ^{5,12}	-	ns	12
ACT to PRE command period			tRAS	32	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	46.25 (45.75) ^{5,12}	-	ns	12
	Normal	Read DBI					
CWL =9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,11
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,9
				(Optional) ^{5,12}			
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,9
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,9
				(Optional) ^{5,12}			
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	1.071	<1.25	ns	1,2,3,9
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,9
				(Optional) ^{5,12}			
CWL = 12,16	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,9
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,9
				(Optional) ^{5,12}			
CWL = 14,18	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3
	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833	ns	1,2,3,4
	CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns	1,2,3
Supported CL Settings				10,(11),12,(13),14,(15),16,(17),18,19,20		nCK	13
Supported CL Settings with read DBI				12,(13),14,(15),16,(18),19,(20),21,22,23		nCK	
Supported CWL Settings				9,10,11,12,14,16,18		nCK	

Note:

Absolute Specification

- VDDQ = VDD = 1.20V +/- 0.06 V
- VPP = 2.5V +0.25/-0.125 V
- The values defined with above-mentioned table are DLL ON case.
- DDR4-1600, 1866, 2133, 2400 and 2666 Speed Bin Tables are valid only when Geardown Mode is disabled.

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(avg) value (1.5, 1.25, 1.071, 0.938, 0.833 or 0.750 ns) when calculating CL [nCK] = tAA [ns] / tCK(avg) [ns], rounding up to the next 'Supported CL', where tAA = 12.5ns and tCK(avg) = 1.3 ns should only be used for CL = 10 calculation.
3. tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.938 ns or 0.833 ns or 0.750 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR4-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. Any DDR4-2666 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
10. Reserved for DDR4-3200 speed bin.
11. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
12. Parameter apply from tCK(avg)min to tCH(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
13. CL number in parentheses, it means that these numbers are optional.
14. DDR4 SDRAM supports CL=9 as long as a system meets tAA(min).

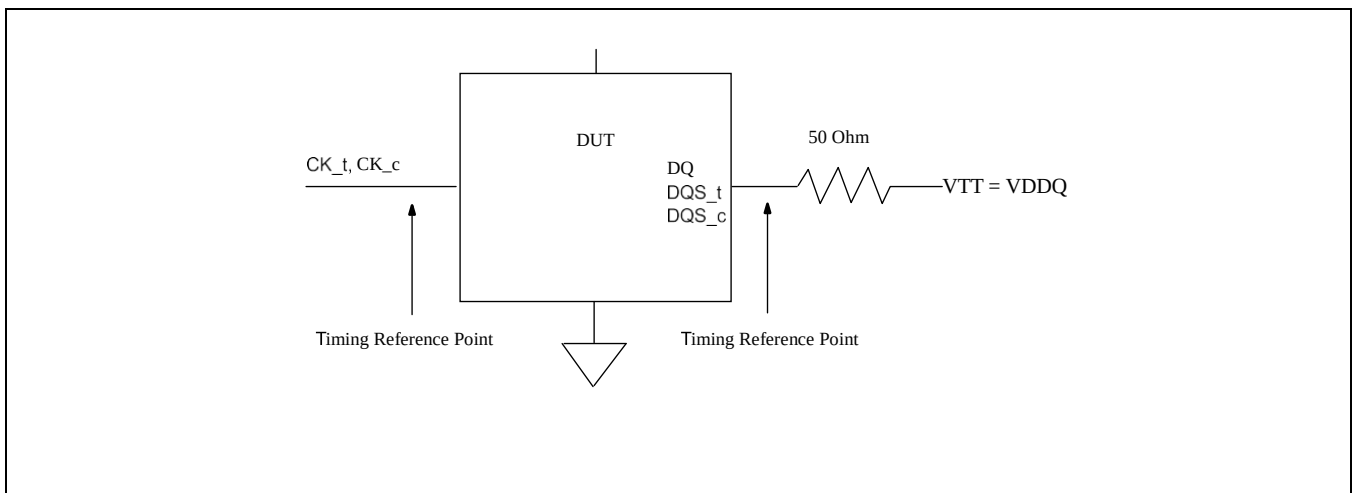
7 Electrical Characteristics & Timing

7.1 Reference Load for AC Timing and Output Slew Rate

Figure 3 represents the effective reference load of 50 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

Figure 3 - Reference Load for AC Timings and Output Slew Rates



7.2 Timing Parameters by Speed Grade

Table 10 - AC Timing parameters

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE	
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
Clock Timing												
Minimum Clock +Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	8	20	8	20	8	20	ns		
Average Clock Period	tCK(avg)	1.25	<1.5	1.071	<1.25	0.938	<1.071	0.833	<0.938	ns	35,36	
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)		
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)		
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_tot	tCK(avg)max + tJIT(per)max_tot	tCK(avg)min + tJIT(per)min_tot	tCK(avg)max + tJIT(per)max_tot	tCK(avg)min + tJIT(per)min_tot	tCK(avg)max + tJIT(per)max_tot	tCK(avg)min + tJIT(per)min_tot	tCK(avg)max + tJIT(per)max_tot	tCK(avg)		
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	23	
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	24	
Clock Period Jitter- total	JIT(per)_tot	-63	63	-54	54	-47	47	-42	42	ps	25	
Clock Period Jitter- deterministic	JIT(per)_dj	-31	31	-27	27	-23	23	-21	21	ps	26	
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-50	50	-43	43	-38	38	-33	33	ps		
Cycle to Cycle Period Jitter	tJIT(cc)_total	125		107		94		83		ps	25	
Cycle to Cycle Period Jitter deterministic	tJIT(cc)_dj	63		54		47		42		ps	26	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	100		86		75		67		ps		
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps		
Cumulative error across 2 cycles	tERR(2per)	-92	92	-79	79	-69	69	-61	61	ps		
Cumulative error across 3 cycles	tERR(3per)	-109	109	-94	94	-82	82	-73	73	ps		
Cumulative error across 4 cycles	tERR(4per)	-121	121	-104	104	-91	91	-81	81	ps		
Cumulative error across 5 cycles	tERR(5per)	-131	131	-112	112	-98	98	-87	87	ps		
Cumulative error across 6 cycles	tERR(6per)	-139	139	-119	119	-104	104	-92	92	ps		
Cumulative error across 7 cycles	tERR(7per)	-145	145	-124	124	-109	109	-97	97	ps		
Cumulative error across 8 cycles	tERR(8per)	-151	151	-129	129	-113	113	-101	101	ps		
Cumulative error across 9 cycles	tERR(9per)	-156	156	-134	134	-117	117	-104	104	ps		
Cumulative error across 10 cycles	tERR(10per)	-160	160	-137	137	-120	120	-107	107	ps		
Cumulative error across 11 cycles	tERR(11per)	-164	164	-141	141	-123	123	-110	110	ps		
Cumulative error across 12 cycles	tERR(12per)	-168	168	-144	144	-126	126	-112	112	ps		
Cumulative error across 13 cycles	tERR(13per)	-172	172	-147	147	-129	129	-114	114	ps		
Cumulative error across 14 cycles	tERR(14per)	-175	175	-150	150	-131	131	-116	116	ps		
Cumulative error across 15 cycles	tERR(15per)	-178	178	-152	152	-133	133	-118	118	ps		
Cumulative error across 16 cycles	tERR(16per)	-180	180	-155	155	-135	135	-120	120	ps		
Cumulative error across 17 cycles	tERR(17per)	-183	183	-157	157	-137	137	-122	122	ps		
Cumulative error across 18 cycles	tERR(18per)	-185	185	-159	159	-139	139	-124	124	ps		
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	$tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min)$ $tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)$									ps	
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	115	-	100	-	80	-	62	-	ps		
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	215	-	200	-	180	-	162	-	ps		
Command and Address hold timeto CK_t, CK_c referenced to Vih(dc) /Vil(dc) levels	tIH(base)	140	-	125	-	105	-	87	-	ps		
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	215	-	200	-	180	-	162	-	ps		
Control and Address Input pulse width for each input	tIPW	600	-	525	-	460	-	410	-	ps		
Command and Address Timing												
CAS_n to CAS_n command delay for same bank group	tCCD_L	Max(5nCK, 6.250ns)	-	Max(5nCK, 5.355ns)	-	Max(5nCK, 5.355ns)	-	Max(5nCK, 5.000ns)	-	nCK	34	

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK, 6ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	Max(4nCK, 5ns)	-	Max(4nCK, 4.2ns)	-	Max(4nCK, 3.7ns)	-	Max(4nCK, 3.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1/ 2KB page size	tRRD_S(1/ 2K)	Max(4nCK, 5ns)	-	Max(4nCK, 4.2ns)	-	Max(4nCK, 3.7ns)	-	Max(4nCK, 3.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK, 7.5ns)	-	Max(4nCK, 6.4ns)	-	Max(4nCK, 6.4ns)	-	Max(4nCK, 6.4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK, 6ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 4.9ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L (1/ 2K)	Max(4nCK, 6ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 4.9ns)	-	nCK	34
Four activate window for 2KB page size	tFAW_2K	Max(28nCK, 35ns)	-	Max(28nCK, 30ns)	-	Max(28nCK, 30ns)	-	Max(28nCK, 30ns)	-	ns	34
Four activate window for 1KB page size	tFAW_1K	Max(20nCK, 25ns)	-	Max(20nCK, 23ns)	-	Max(20nCK, 21ns)	-	Max(20nCK, 21ns)	-	ns	34
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK, 20ns)	-	Max(16nCK, 17ns)	-	Max(16nCK, 15ns)	-	Max(16nCK, 13ns)	-	ns	34
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max(2nCK, 2.5ns)	-	max(2nCK, 2.5ns)	-	max(2nCK, 2.5ns)	-	max (2nCK, 2.5ns)	-		1, 2, 34
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-		1,34
Internal READ Command to PRE-CHARGE Command delay	tRTP	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	Max(4nCK, 7.5ns)	-		
WRITE recovery time	tWR	15	-	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR+max (4nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	ns	1, 28
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	tWTR_S_C RC_DM	tWTR_S+max (4nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	ns	2, 29, 34
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_C RC_DM	tWTR_L+max (4nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	ns	3,30 34
DLL locking time	tDLLK	597	-	597	-	768	-	768	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	8	-	nCK	
Mode Register Set command update delay	tMOD	max(24nCK, 15ns)	-	max(24nCK, 15ns)	-	max(24nCK, 15ns)	-	max(24nCK, 15ns)	-		
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	1	-	nCK	33
Multi Purpose Register Write Recovery Time	tWR_MPR	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	-	
Auto precharge write recovery + pre-charge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))								nCK	
CS_n to Command Address Latency											
CS_n to Command Address Latency	tCAL	3	-	4	-	4	-	5	-	nCK	
DRAM Data Timing											
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	0.16	-	0.16	-	0.16	-	0.17	tCK(avg) /2	13,18
DQ output hold time from DQS_t,DQS_c	tQH	0.76	-	0.76	-	0.76	-	0.74	-	tCK(avg) /2	13,17, 18

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
DQS_t, DQS_c differential READ Preamble(1 clock preamble)	tRPRE	0.9	-	0.9	-	0.9	-	0.9	-	tCK	
DQS_t, DQS_c differential READ Preamble(2 clock preamble)	tRPRE2	1.8	-	1.8	-	1.8	-	1.8	-	tCK	
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	-	0.33	-	0.33	-	0.33	-	tCK	
DQS_t,DQS_c differential output high time	tQSH	0.4	-	0.4	-	0.4	-	0.4	-	tCK	21
DQS_t,DQS_c differential output low time	tQSL	0.4	-	0.4	-	0.4	-	0.4	-	tCK	20
DQS_t, DQS_c differential WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	tCK	
DQS_t, DQS_c differential WRITE Preamble(2 clock preamble)	tWPRE2	NA	-	NA	-	NA	-	1.8	-	tCK	
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	-	0.33	-	0.33	-	0.33	-	tCK	
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-450	225	-390	195	-360	180	-300	150	ps	
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	225	-	195	-	180	-	150	ps	
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c rising edge output timing locatino from rising CK_t, CK_c with DLL On mode	tDQSCK	-225	225	-195	195	-180	180	-175	175	ps	
Command Path Timing											
Command path disable delay upon MPSM entry	tMPED	MIN = tMOD(min) + tCPDED(min)								tCK	
Valid clock requirement after MPSM entry	tCKMPE	MIN = tMOD(min) + tCPDED(min)								tCK	
Valid clock requirement before MPSM exit	tCKMPX	MIN = tCKSRX(min)								tCK	
Exit MPSM to commands not requir- ing a locked DLL	tXMP	MIN = tXS(min)								tCK	
Exit MPSM to commands requiring a locked DLL	tXMPDLL	MIN = tXMP(min) + tXSDDL(mi								tCK	
CS setup time to CKE	tMPX_S	MIN = tIS(min) + tIH(min)								ns	
CS_n High hold time to CKE rising edge	tMPX_HH	MIN = tXP(min)								ns	
CS_n Low hold time to CKE rising edge	tMPX_LH	12	tXMP-10ns	12	tXMP-10ns	12	tXMP-10ns	12	tXMP-10ns	ns	
Calibration Timing											
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	128	-	nCK	
Reset/Self Refresh Timing											
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK,tRFC(min)+ 10ns)	-	max (5nCK,tRFC(min)+ 10ns)	-	max (5nCK,tRFC(min)+ 10ns)	-	max (5nCK,tRFC(min)+ 10ns)	-		
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+ 10ns	-	tRFC(min)+ 10ns	-	tRFC(min)+ 10ns	-	tRFC(min)+ 10ns	-		
SRX to commands not requiring a locked DLL in Self RefreshABORT	tX-S_ABORT(min)	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-		
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST(min)	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-		
Exit Self Refresh to commands re- quiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-		
Minimum CKE low width for Self re- fresh entry to exit timing	tCKESR	tCKE(min)+1 nCK	-	tCKE(min)+1 nCK	-	tCKE(min)+1 nCK	-	tCKE(min)+1 nCK	-		
Minimum CKE low width for Self re- fresh entry to exit timing with CA Par- ity enabled	tCKESR_PAR	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-		

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK,10 ns)	-	max(5nCK,10 ns)	-	max(5nCK,10 ns)	-	max(5nCK,10ns)	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKS-RE_PAR	max(5nCK,10ns)+PL	-	max(5nCK,10ns)+PL	-	max(5nCK,10ns)+PL	-	max(5nCK,10ns)+PL	-		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK,10 ns)	-	max(5nCK,10 ns)	-	max(5nCK,10 ns)	-	max(5nCK,10ns)	-		
Power Down Timing											
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(4nCK,6ns)	-	max(4nCK,6ns)	-	max(4nCK,6ns)	-	max(4nCK,6ns)	-		
CKE minimum pulse width	tCKE	max(3nCK, 5ns)	-	max(3nCK, 5ns)	-	max(3nCK, 5ns)	-	max(3nCK, 5ns)	-		31,32
Command pass disable delay	tCPDED	4	-	4	-	4	-	4	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI		6
Timing of ACT command toPower Down entry	tACTPDEN	1	-	1	-	2	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	2	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRP-BC4DEN	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAP-BC4DEN	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	nCK	5
Timing of REF command toPower Down entry	tREFPDEN	1	-	1	-	2	-	2	-	nCK	7
Timing of MRS command toPower Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-		
PDA Timing											
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK, 10ns)		max(16nCK, 10ns)		max(16nCK, 10ns)		max(16nCK, 10ns)			
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD		tMOD			
ODT Timing											
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	
Write Leveling Timing											
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	40	-	nCK	12
DQS_t/DQS_n delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_c crossing	tWLH	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE									ns	
CA Parity Timing											
Commands not guaranteed to be executed during this time	tPAR_UNKNOWN	-	PL	-	PL	-	PL	-	PL		

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Delay from errant command to ALERT_n assertion	tPAR_ALER T_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns		
Pulse width of ALERT_n signal when asserted	tPAR_ALER T_PW	48	96	56	112	64	128	72	144	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALER T_RSP	-	43	-	50	-	57	-	64	nCK	
Parity Latency	PL	4		4		4		5		nCK	
CRC Error Reporting											
CRC error to ALERT_nlatency	tCRC_ALER T	3	13	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	tCRC_ALER T_PW	6	10	6	10	6	10	6	10	nCK	
tREFI											
tRFC1 (min)	2Gb	160	-	160	-	160	-	160	-	ns	34
	4Gb	260	-	260	-	260	-	260	-	ns	34
	8Gb	350	-	350	-	350	-	350	-	ns	34
	16Gb	550	-	550	-	550	-	550	-	ns	34
tRFC2 (min)	2Gb	110	-	110	-	110	-	110	-	ns	34
	4Gb	160	-	160	-	160	-	160	-	ns	34
	8Gb	260	-	260	-	260	-	260	-	ns	34
	16Gb	350	-	350	-	350	-	350	-	ns	34
tRFC4 (min)	2Gb	90	-	90	-	90	-	90	-	ns	34
	4Gb	110	-	110	-	110	-	110	-	ns	34
	8Gb	160	-	160	-	160	-	160	-	ns	34
	16Gb	260	-	260	-	260	-	260	-	ns	34

Table 11 - AC Timing parameters for DDR4-2666

Speed		DDR4-2666		Units	NOTE
Parameter	Symbol	MIN	MAX		
Clock Timing					
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	ns	
Average Clock Period	tCK(avg)	0.750	<0.833	ns	35,36
Average high pulse width	tCH(avg)	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_tot	tCK(avg)max + tJIT(per)max_tot	tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	tCK(avg)	24
Clock Period Jitter- total	JIT(per)_tot	-38	38	ps	25
Clock Period Jitter- deterministic	JIT(per)_dj	-19	19	ps	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-30	30	ps	
Cycle to Cycle Period Jitter	tJIT(cc)_total	75		ps	25
Cycle to Cycle Period Jitter deterministic	tJIT(cc)_dj	38		ps	26
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	60		ps	
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	ps	
Cumulative error across 2 cycles	tERR(2per)	-55	55	ps	
Cumulative error across 3 cycles	tERR(3per)	-66	66	ps	
Cumulative error across 4 cycles	tERR(4per)	-73	73	ps	
Cumulative error across 5 cycles	tERR(5per)	-78	78	ps	
Cumulative error across 6 cycles	tERR(6per)	-83	83	ps	
Cumulative error across 7 cycles	tERR(7per)	-87	87	ps	
Cumulative error across 8 cycles	tERR(8per)	-91	91	ps	
Cumulative error across 9 cycles	tERR(9per)	-94	94	ps	
Cumulative error across 10 cycles	tERR(10per)	-96	96	ps	
Cumulative error across 11 cycles	tERR(11per)	-99	99	ps	
Cumulative error across 12 cycles	tERR(12per)	-101	101	ps	
Cumulative error across 13 cycles	tERR(13per)	-103	103	ps	
Cumulative error across 14 cycles	tERR(14per)	-104	104	ps	
Cumulative error across 15 cycles	tERR(15per)	-106	106	ps	
Cumulative error across 16 cycles	tERR(16per)	-108	108	ps	
Cumulative error across 17 cycles	tERR(17per)	-110	110	ps	
Cumulative error across 18 cycles	tERR(18per)	-112	112	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)		ps	
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	55	-	ps	
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	145	-	ps	
Command and Address hold timeto CK_t, CK_c referenced to Vih(dc) /Vil(dc) levels	tIH(base)	80	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	145	-	ps	
Control and Address Input pulse width for each input	tIPW	385	-	ps	
Command and Address Timing					
CAS_n to CAS_n command delay for same bank group	tCCD_L	Max(5nCK, 5.000ns)	-	nCK	34

Speed		DDR4-2666		Units	NOTE
Parameter	Symbol	MIN	MAX		
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK, 5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1KB page size	tRRD_S(1K)	Max(4nCK, 3 ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1/ 2KB page size	tRRD_S(1/ 2K)	Max(4nCK, 3 ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK, 6.4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK, 4.9ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L (1/ 2K)	Max(4nCK, 4.9ns)	-	nCK	34
Four activate window for 2KB page size	tFAW_2K	Max(28nCK, 30ns)	-	ns	34
Four activate window for 1KB page size	tFAW_1K	Max(20nCK, 21ns)	-	ns	34
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK, 12ns)	-	ns	34
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max (2nCK, 2.5ns)	-	ns	1,2, 34
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nCK, 7.5ns)	-	ns	1,34
Internal READ Command to PRE-CHARGE Command delay	tRTP	Max(4nCK, 7.5ns)	-	ns	34
WRITE recovery time	tWR	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR+max (5nCK, 3.75ns)	-	ns	1, 28
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	tWTR_S_C RC_DM	tWTR_S+max (5nCK, 3.75ns)	-	ns	2, 29, 34
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_C RC_DM	tWTR_L+max (5nCK, 3.75ns)	-	ns	3,30, 34
DLL locking time	tDLLK	854	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	nCK	
Mode Register Set command update delay	tMOD	max(24nCK, 15ns)	-	nCK	37
Multi-Purpose Register Recovery Time	tMPRR	1	-	nCK	33
Multi Purpose Register Write Recovery Time	tWR_MPR	tMOD (min) + AL + PL	-	nCK	
Auto precharge write recovery + pre-charge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))		nCK	
CS_n to Command Address Latency					
CS_n to Command Address Latency	tCAL	5	-	nCK	
DRAM Data Timing					
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	0.18	tCK(avg) /2	13,18
DQ output hold time from DQS_t,DQS_c	tQH	0.74	-	tCK(avg) /2	13,17, 18

Speed		DDR4-2666		Units	NOTE
Parameter	Symbol	MIN	MAX		
DQS_t, DQS_c differential READ Preamble(1 clock preamble)	tRPRE	0.9	-	tCK	
DQS_t, DQS_c differential READ Preamble(2 clock preamble)	tRPRE2	1.8	-	tCK	
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	-	tCK	
DQS_t, DQS_c differential output high time	tQSH	0.4	-	tCK	21
DQS_t, DQS_c differential output low time	tQSL	0.4	-	tCK	20
DQS_t, DQS_c differential WRITE Preamble	tWPRE	0.9	-	tCK	
DQS_t, DQS_c differential WRITE Preamble(2 clock preamble)	tWPRE2	1.8	-	tCK	
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	-	tCK	
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-310	170	ps	
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	170	ps	
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	tCK	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	tCK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	tCK	
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	tCK	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	tCK	
DQS_t, DQS_c rising edge output timing locatino from rising CK_t, CK_c with DLL On mode	tDQSCK	-170	170	ps	
MPSM Timing					
Command path disable delay upon MPSM entry	tMPED	tMOD (MIN) + tCPDED (MIN)	-	nCK	
Valid clock requirement after MPSM entry	tCKMPE	tMOD (MIN) + tCPDED (MIN)	-	nCK	
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX (MIN)	-	nCK	
Exit MPSM to commands not requiring a locked DLL	tXMP	tXS (MIN)	-	nCK	
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP (MIN) + tXSDLL (MIN)	-	nCK	
CS setup time to CKE	tMPX_S	tIS (MIN) + tIH (MIN)	-	ns	
CS_n High hold time to CKE rising edge	tMPX_HH	tXP	-	ns	
CS_n Low hold time to CKE rising edge	tMPX_LH	12	tXMP-10ns	ns	
Calibration Timing					
Power-up and RESET calibration time	tZQinit	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	nCK	
Reset/Self Refresh Timing					
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK, tRFC(min)+ 10ns)		nCK	
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+ 10ns	-	nCK	
SRX to commands not requiring a locked DLL in Self RefreshABORT	tX-S_ABORT(min)	tRFC4(min)+ 10ns	-	nCK	
Exit Self Refresh to ZQCL, ZQCS and MRS (CL, CWL, WR, RTP and Gear Down)	tXS_FAST(min)	tRFC4(min)+ 10ns	-	nCK	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+1 nCK	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKESR_PAR	tCKE(min)+ 1nCK+PL	-	nCK	

Speed		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max (5nCK,10ns)	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKS-RE_PAR	max (5nCK,10ns)+PL	-	nCK	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max (5nCK,10ns)	-	nCK	
Power Down Timing					
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (4nCK,6ns)	-	nCK	
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	nCK	31,32
Command pass disable delay	tCPDED	4	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	nCK	6
Timing of ACT command toPower Down entry	tACTPDEN	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRP-BC4DEN	WL+2+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAP-BC4DEN	WL+2+WR+1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	nCK	
PDA Timing					
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK, 10ns)		nCK	
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		nCK	
ODT Timing					
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	ns	
RTT dynamic change skew	tADC	0.3	0.7	tCK(avg)	
Write Leveling Timing					
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	nCK	12
DQS_t/DQS_n delay after write leveling mode is programmed	tWLDQSEN	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_c crossing	tWLH	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	ns	
Write leveling output error	tWLOE	0	2	ns	
CA Parity Timing					
Commands not guaranteed to be executed during this time	tPAR_UNKNOWN	-	PL	nCK	

Speed		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX		
Delay from errant command to ALERT_n assertion	tPAR_ALE R T_ON	-	PL+6ns	nCK	
Pulse width of ALERT_n signal when asserted	tPAR_ALE R T_PW	80	160	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALER T_RSP	-	71	nCK	
Parity Latency	PL	5		nCK	
CRC Error Reporting					
CRC error to ALERT_nlatency	tCRC_ALER T	3	13	ns	
CRC ALERT_n pulse width	CRC_ALER T_PW	6	10	nCK	
Geardown setup time	tGEAR_setup	2	-	nCK	
Geardown hold time	tGEAR_hold	2	-	nCK	
tREFI					
tRFC1 (min)	2Gb	160	-	ns	34
	4Gb	260	-	ns	34
	8Gb	350	-	ns	34
	16Gb	550	-	ns	34
tRFC2 (min)	2Gb	110	-	ns	34
	4Gb	160	-	ns	34
	8Gb	260	-	ns	34
	16Gb	350	-	ns	34
tRFC4 (min)	2Gb	90	-	ns	34
	4Gb	110	-	ns	34
	8Gb	160	-	ns	34
	16Gb	260	-	ns	34

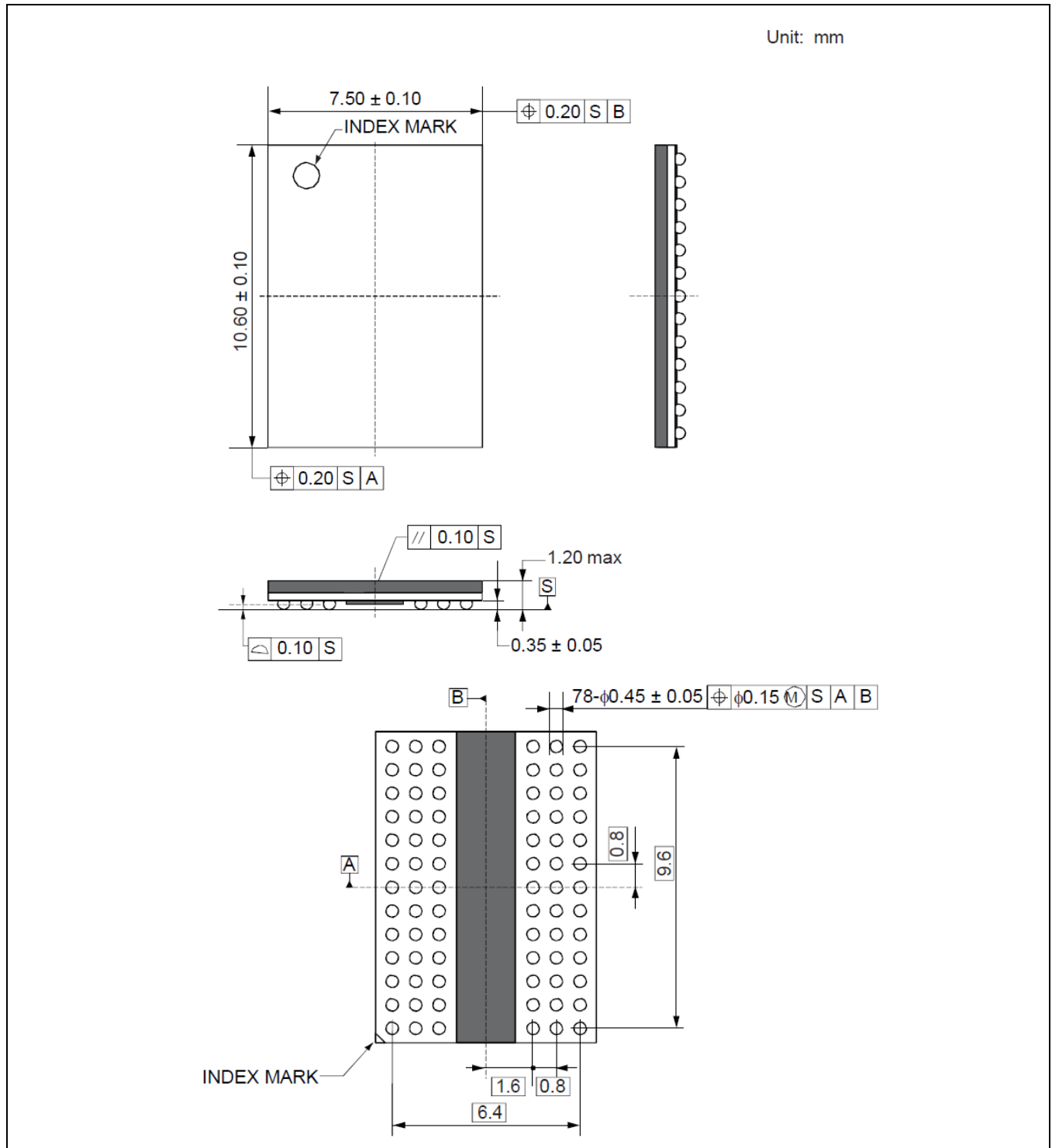
Note:

1. Start of internal write transaction is defined as follows:
For BL8 (Fixed by MRS and on the-fly): Rising clock edge 4 clock cycles after WL.
For BC4 (on the-fly): Rising clock edge 4 clock cycles after WL.
For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled
3. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
4. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.
5. WR in clock cycles as programmed in MR0.
6. tREFI depends on TCASE
7. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power down IDD spec will not be applied until finishing those operations.
8. For these parameters, the DDR4 SDRAM device supports $t_{nPARAM}[nCK] = RU\{t_{PARAM}[ns]/t_{CK}(avg)[ns]\}$, which is in clock cycles assuming all input clock jitter specifications are satisfied.
9. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR
10. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
11. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
12. The max values are system dependent.
13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are TBD.
14. The deterministic component of the total timing. Measurement method TBD.
15. DQ to DQ static offset relative to strobe per group. Measurement method TBD.
16. This parameter will be characterized and guaranteed by design.
17. When the device is operated with the input clock jitter, this parameter needs to be derated by the actual $t_{jit(per)}_{total}$ of the input clock.(output deratings are relative to the SDRAM input clock).Example TBD.
18. DRAM DBI mode is off.
19. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20. tQSL describes the instantaneous differential output low pulse width on DQS_tDQS_c, as measured from on falling edge to the next.
21. tQSH describes the instantaneous differential output high pulse width on DQS_tDQS_c, as measured from on falling edge to the next consecutive rising edge.
22. There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI.
23. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
24. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are TBD.
26. The deterministic jitter component out of the total jitter. This parameter is characterized and guaranteed by design.
27. This parameter has to be even number of clocks
28. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
29. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWT
30. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
31. After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).
32. After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification (HIGH pulse width).
33. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
34. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
35. This parameter must keep consistency with Speed Bin Tables shown in section 10.
36. DDR4 1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate. $UI = t_{CK}(avg).min/2$
37. For MR7 commands, the minimum delay to a subsequent non -MRS command is 5nCK.

8 Package Outlines

Figure 4 reflects the current status of the outline dimensions of the DDR4 packages for 4Gbit components configuration.

Figure 4 - Package outline(78ball FBGA)



[illegible]

9 Product Type Nomenclature

For reference the UnilC SDRAM component nomenclature is enclosed in this chapter

Table 12 - DDR4 Memory Components

Field	Description	Values	Coding
1	UnilC Component Prefix	SCB	UnilC
2	Voltage	12	VDD, VDDQ=1.14V-1.26V
3	DRAM Technology	Q	DDR4
4	Density	4G	4 Gbit
5	Number of I/Os	80	X8
		16	X16
6	Product Variant	0 .. 9	–
7	Die Revision	A	First
		B	Second
		C	Third
8	Package,	F	FBGA Green
9	Power	–	Standard power product
		L	Low power product
10	Speed Grade	07Q	CL–tRCD–tRP =19-19-19
		08T	CL–tRCD–tRP =17-17-17

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