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16Gbit LPDDR4X SDRAM

EU RoHS Compliant Products

Data Sheet

Rev. B

Revision History		
Date	Revision	Subjects (major changes since last revision)
2024-04	A	First version release
2024-12	B	Update 16Gb only, IDD

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1 General Specification

1.1 Product List

Table 1 - LPDDR4X Device Information

Part Number	Density	Organization	Data Rate(Mbps)	Package
SCB11R16322CF-04Z	16Gb	X32	4266	BGA200
SCB11R16322CF-03A	16Gb	X32	3733	BGA200

1.2 Address Table

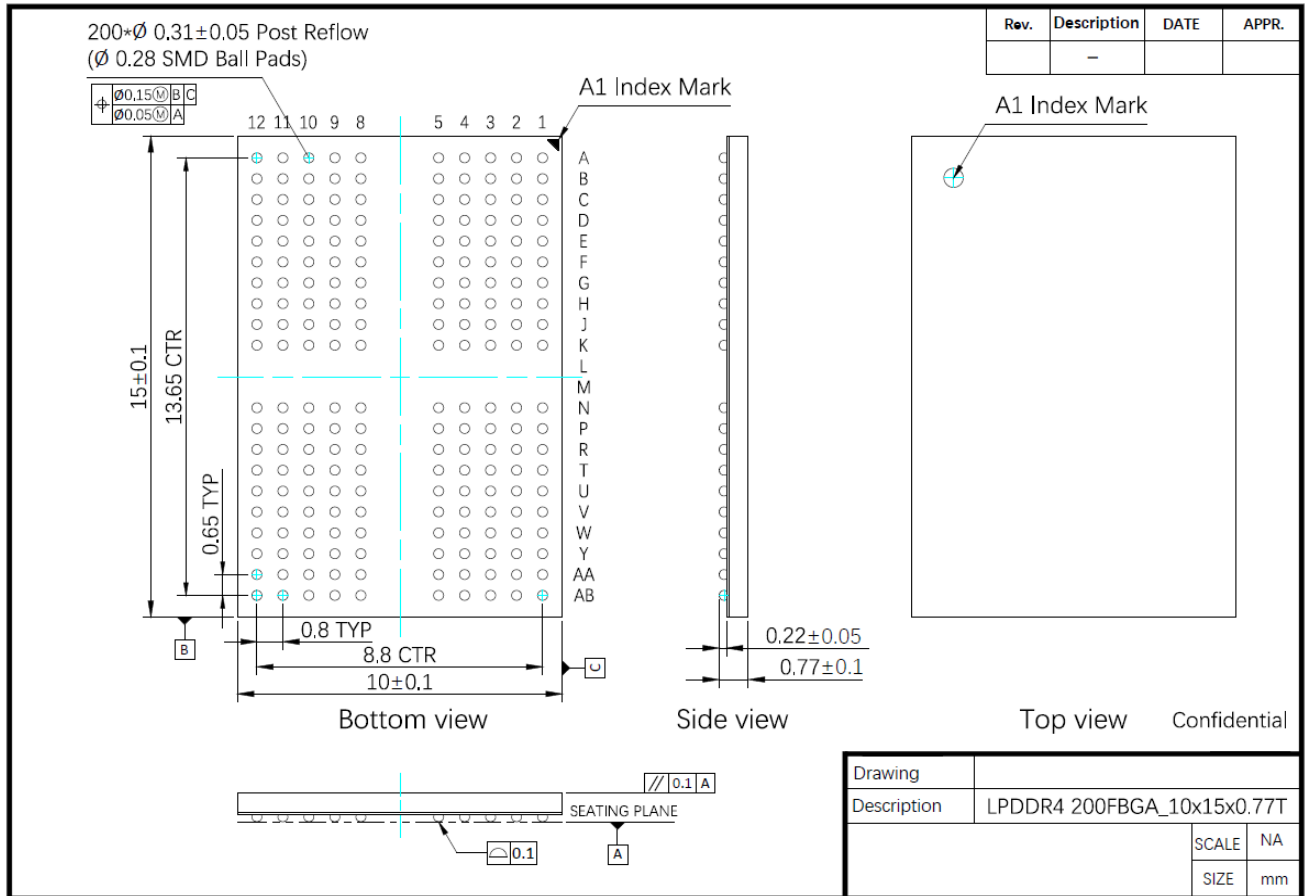
Table 2 - Die Addressing Table

Die Configuration	512Mb x16
Bank Address	BA0~BA2
Row Address	A0~A15
Column Address	A0~A9

2 Package Information

2.1 200-Ball x32 Discrete Package Dimension

Figure 1 - 200-Ball x32 Discrete FBGA Package Dimension



2.2 x32 Discrete Package Ballout

Figure 2 - x32 Discrete Package Ballout

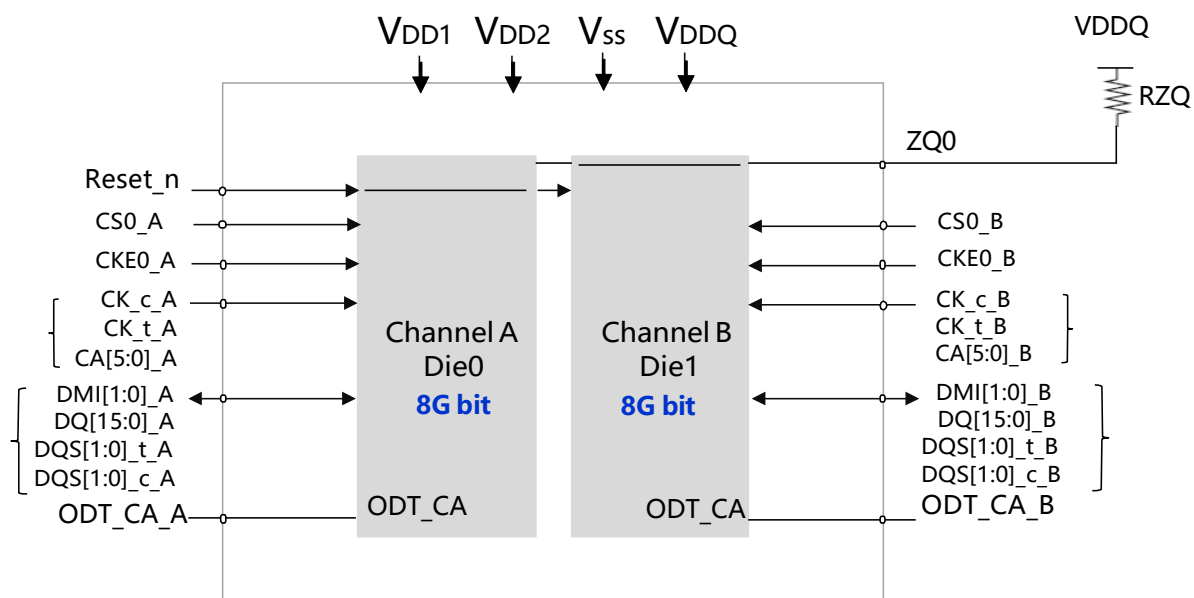
	1	2	3	4	5	6	7	8	9	10	11	12
A	DNU	DNU	VSS	VDD2	ZQ0			ZQ1	VDD2	VSS	DNU	DNU
B	DNU	DQ0_A	VDDQ	DQ7_A	VDDQ			VDDQ	DQ15_A	VDDQ	DQ8_A	DNU
C												
D	VSS	DQ1_A	DM10_A	DQ6_A	VSS			VSS	DQ14_A	DM11_A	DQ9_A	VSS
E	VDDQ	VSS	DQS0_t_A	VSS	VDDQ			VDDQ	VSS	DQS1_t_A	VSS	VDDQ
F	VSS	DQ2_A	DQS0_c_A	DQ5_A	VSS			VSS	DQ13_A	DQS1_c_A	DQ10_A	VSS
G	VDD1	DQ3_A	VDDQ	DQ4_A	VDD2			VDD2	DQ12_A	VDDQ	DQ11_A	VDD1
H	VSS	ODTCA_A	VSS	VDD1	VSS			VSS	VDD1	VSS	ZQ2	VSS
J	VDD2	CA0_A	CS1_A	CS0_A	VDD2			VDD2	CA2_A	CA3_A	CA4_A	VDD2
K	VSS	CA1_A	VSS	CKE0_A	CKE1_A			CK_t_A	CK_c_A	VSS	CA5_A	VSS
L	VDD2	VSS	VDD2	VSS	CS2_A			CKE2_A	VSS	VDD2	VSS	VDD2
M												
N	VDD2	VSS	VDD2	VSS	CS2_B			CKE2_B	VSS	VDD2	VSS	VDD2
P	VSS	CA1_B	VSS	CKE0_B	CKE1_B			CK_t_B	CK_c_B	VSS	CA5_B	VSS
R	VDD2	CA0_B	CS1_B	CS0_B	VDD2			VDD2	CA2_B	CA3_B	CA4_B	VDD2
T	VSS	ODTCA_B	VSS	VDD1	VSS			VSS	VDD1	VSS	RESET_n	VSS
U	VDD1	DQ3_B	VDDQ	DQ4_B	VDD2			VDD2	DQ12_B	VDDQ	DQ11_B	VDD1
V	VSS	DQ2_B	DQS0_c_B	DQ5_B	VSS			VSS	DQ13_B	DQS1_c_B	DQ10_B	VSS
W	VDDQ	VSS	DQS0_t_B	VSS	VDDQ			VDDQ	VSS	DQS1_t_B	VSS	VDDQ
Y	VSS	DQ1_B	DM10_B	DQ6_B	VSS			VSS	DQ14_B	DM11_B	DQ9_B	VSS
AA	DNU	DQ0_B	VDDQ	DQ7_B	VDDQ			VDDQ	DQ15_B	VDDQ	DQ8_B	DNU
AB	DNU	DNU	VSS	VDD2	VSS			VSS	VDD2	VSS	DNU	DNU

Note:

- 0.8mm pitch (X-axis), 0.65mm pitch (Y-axis), 22 rows using MO-311 0.80mm Pitch
- Top View, A1 in top left corner. CS1_A/B, CE1_A/B, ZQ1 is floating for 2GB package.
- ODT(ca)_[x] balls are wired to ODT(ca)_[x] pads of Rank 0 DRAM die. ODT(ca)_[x] pads for other ranks (if present) are disabled in the package.
- ZQ2, CKE2_A, CKE2_B, CS2_A, and CS2_B balls are reserved for 3-rank package. For 1-rank and 2-rank package those balls are NC.
- Die pad VSS and VSSQ signals are combined to VSS package balls.
- Package requires dual channel die or functional equivalent of single channel die-stack.

2.3 Block Diagram

Figure 3 - Dual-Die, Dual-Channel, Single-Rank Package Block Diagram (2GB x32 I/O)



2.4 Ball Definition

“_A” and “_B” indicate DRAM channels. “_A” balls are present in all devices while “_B” balls are present in dual channel SDRAM devices only. LPDDR4X ball definitions are the same as LPDDR4, except ODT_CA pins as described in Table 3.

Table 3 - Ball Definition

Symbol	Type	Description
CK_t_A, CK_c_A, CK_t_B, CK_c_B	Input	Clock: CK_t and CK_c are differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to CK. Each channel (A & B) has its own clock pair.
CKE_A, CKE_B	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is part of the command code. Each channel (A & B) has its own CKE signal.
CS_A, CS_B	Input	Chip Select: CS is part of the command code. Each channel (A & B) has its own CS signal.
CA[5:0]_A, CA[5:0]_B	Input	Command/Address Inputs: CA signals provide the Command and Address inputs according to the Command Truth Table. Each channel (A&B) has its own CA signals.
DQ[15:0]_A, DQ[15:0]_B	I/O	Data Input/Output: Bi-direction data bus.
DQS[1:0]_t_A, DQS[1:0]_c_A, DQS[1:0]_t_B, DQS[1:0]_c_B	I/O	Data Strobe: DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and must arrive prior to Data. Each byte of data has a Data Strobe signal pair. Each channel (A & B) has its own DQS strobes.
DMI[1:0]_A, DMI[1:0]_B	I/O	Data Mask Inversion: DMI is a bi-directional signal which is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. Data Inversion can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel (A & B) has its own DMI signals. This signal is also used along with the DQ signals to provide write data masking information to the DRAM. The DMI pin function - Data Inversion or Data mask - depends on Mode Register setting.
ZQ	Reference	Calibration Reference: Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to VDDQ through a $240\Omega \pm 1\%$ resistor.
VDDQ, VDD1, VDD2	Supply	Power Supplies: Isolated on the die for improved noise immunity.
VSS, VSSQ	GND	Ground Reference: Power supply ground reference
RESET_n	Input	RESET: When asserted LOW, the RESET_n signal resets all channels of the die. There is one RESET_n pad per die.
ODT_CA_A, ODT_CA_B	Input	CA ODT Control: LPDDR4: The ODT_CA pin is used in conjunction with the Mode Register to turn on/off the On-Die-Termination for CA pins. LPDDR4X: The ODT_CA pin is ignored by LPDDR4X devices. ODT_CS/CA/CK Function is fully controlled through MR11 and MR22. The ODT_CA pin shall be connected to either VDD2 or Vss.

3 Absolute Maximum DC Ratings

This chapter specifies absolute maximum DC ratings. Stresses greater than those listed may cause permanent damage to the device.

This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 4 - Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Unit
VDD1 supply voltage relative to VSS ¹	VDD1	-0.4	2.1	V
VDD2 supply voltage relative to VSS ¹	VDD2	-0.4	1.5	
VDDQ supply voltage relative to VSSQ ¹	VDDQ			
Voltage on any ball except VDD1 relative to VSS	V _{IN} , V _{OUT}			
Storage Temperature ²	T _{STG}	-55	125	°C

Note:

- See "Power-Ramp" for relationships between power supplies.
- Storage temperature is the case surface temperature on the center/top side of the LPDDR4X device. For the measurement conditions, please refer to JEDEC51-2.

4 AC and DC Operating Conditions

This chapter points out four key conditions for low power device working reliably, safely and legally, which are DC operating voltage, input/output leakage current, temperature, single-ended and differential output slew rate.

4.1 Recommended DC Operating Conditions for Low Voltage

Table 5 - LPDDR4 Recommended DC Operating Conditions

DRAM	Symbol	Min	Typ	Max	Unit	Note
Core 1 Power	VDD1	1.7	1.8	1.95	V	1,2
Core 1 Power/Input Buffer Power	VDD2	1.06	1.1	1.17	V	1,2,3
I/O Buffer Power	VDDQ	1.06	1.1	1.17	V	2,3

Note:

- VDD1 uses significantly less current than VDD2.
- The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 20 MHz at the DRAM package ball.
- VdIVW and TdIVW limits described elsewhere in this document apply for voltage noise on supply voltages of up to 45 mV (peak-to-peak) from DC to 20MHz.

Table 6 - LPDDR4X Recommended DC Operating Conditions

DRAM	Symbol	Min	Typ	Max	Unit	Note
Core 1 Power	VDD1	1.7	1.8	1.95	V	1,2
Core 1 Power/Input Buffer	VDD2	1.06	1.1	1.17	V	1,2,3
I/O Buffer Power	VDDQ	0.57	0.6	0.65	V	2,3,4,5

Note:

- VDD1 uses significantly less current than VDD2.
- The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 20 MHz at the DRAM package ball.
- The voltage noise tolerance from DC to 20 MHz exceeding a pk-pk tolerance of 45 mV at the DRAM ball is not included in the TdIVW.

- 4 VDDQ(max) may be extended to 0.67 V as an option in case the operating clock frequency is equal or less than 800 Mhz.
- 5 Pull up, pull down and ZQ calibration tolerance spec is valid only in normal VDDQ tolerance range (0.57V-0.65V).

4.2 Input Leakage Current

Table 7 - Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit
Input Leakage current ^{1,2}	I_L	-4	4	uA

Note:

- 1 For CK_t,CK_c,CKE,CS,CA,ODT_CA and RESET_n. Any input $0V \leq V_{IN} \leq VDD2$ (All other pins not under test = 0V).
- 2 CA ODT is disabled for CK_t,CK_c,CS and CA.

4.3 Input/Output Leakage Current

Table 8 - Input/Output Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit
Input/Output Leakage current ^{1,2}	I_{OZ}	-5	5	uA

Note:

- 1 For DQ, DQS_t, DQS_c and DMI. Any I/O $0V \leq V_{OUT} \leq VDDQ$.
- 2 I/Os status are disabled: High Impedance and ODT Off.

4.4 Operating Temperature Range

Table 9 - Operating Temperature Range

Parameter/Condition	Parameter/Condition	Min	Max	Unit
Standard	T_{OPER}	-25	85	°C
Elevated		85	105	°C

Note:

- 1 Operating Temperature is the case surface temperature on the center-top side of the LPDDR4 device. For the measurement conditions, please refer to JESD51-2.
- 2 Some applications require operation of LPDDR4 in the maximum temperature conditions in the Elevated Temperature Range between 85 °C and 105 °C case temperature. For LPDDR4 devices, derating may be necessary to operate in this range. See MR4.
- 3 Either the device case temperature rating or the temperature sensor may be used to set an appropriate refresh rate, determine the need for AC timing derating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the T_{OPER} rating that applies for the Standard or Elevated Temperature Ranges. For example, T_{CASE} may be above 85 °C when the temperature sensor indicates a temperature of less than 85 °C.

4.5 Single Ended Output Slew Rate

Figure 4 - Single Ended Output Slew Rate Definition

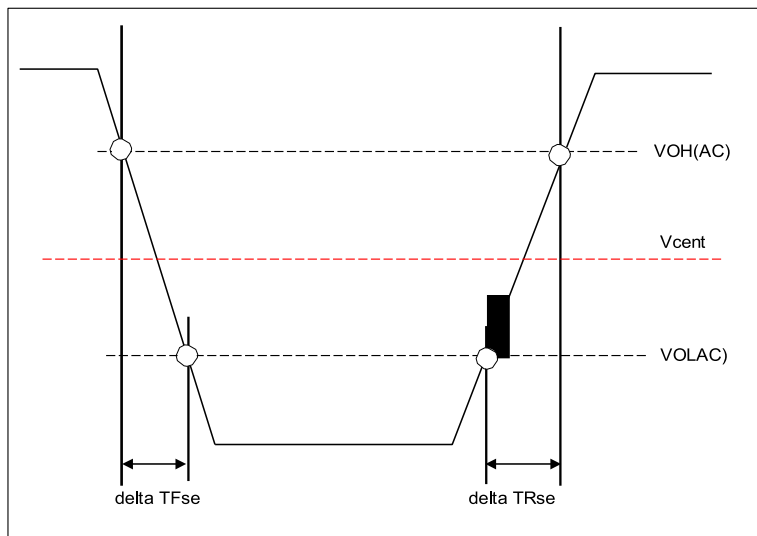


Table 10 - LPDDR4 Output Slew Rate (Single-ended)

Parameter	Symbol	Value		Unit
		Min	Max	
Single-ended Output Slew Rate ($VOH = VDDQ/3$)	SRQ_{se}^a	3.5	9	V/ns
Output slew-rate matching Ratio (Rise to Fall)	-	0.8	1.2	-

^aSR: Slew Rate, Q: Query Output (like in DQ, which stands for Data-in, Query-Output), se: Single-ended Signals

Note:

- 1 Measured with output reference load.
- 2 The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
- 3 The output slew rate for falling and rising edges is defined and measured between $VOL(AC) = 0.2 \cdot VOH(DC)$ And $VOH(AC) = 0.8 \cdot VOH(DC)$.
- 4 Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

Table 11 - LPDDR4X Output Slew Rate (Single-ended) for 0.6V VDDQ

Parameter	Symbol	Value		Unit
		Min	Max	
Single-ended Output Slew Rate ($VOH = VDDQ \cdot 0.5$)	SRQ_{se}^a	3.0	9	V/ns
Output slew-rate matching Ratio (Rise to Fall)	-	0.8	1.2	-

^aSR: Slew Rate, Q: Query Output (like in DQ, which stands for Data-in, Query-Output), se: Single-ended Signals

Note:

- 1 Measured with output reference load.
- 2 The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
- 3 The output slew rate for falling and rising edges is defined and measured between $VOL(AC) = 0.2 \cdot VOH(DC)$ And $VOH(AC) = 0.8 \cdot VOH(DC)$.
- 4 Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

4.6 Differential Output Slew Rate

Figure 5 - Differential Output Slew Rate Definition

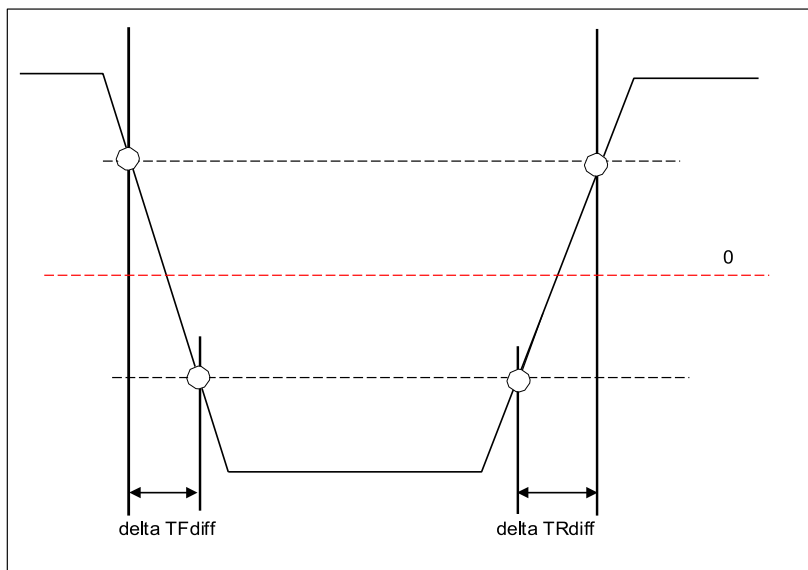


Table 12 - LPDDR4X Differential Output Slew Rate

Parameter	Symbol	Value		Unit
		Min	Max	
Differential Output Slew Rate ($V_{OH} = V_{DDQ}/3$)	SR_{Qdiff}^a	7	18	V/ns
^a SR: Slew Rate, Q: Query Output (like in DQ, which stands for Data-in, Query-Output), diff: differential Signals				

Note:

- 1 Measured with output reference load.
- 2 The output slew rate for falling and rising edges is defined and measured between $V_{OL}(AC) = -0.8 \cdot V_{OH}(DC)$ And $V_{OH}(AC) = 0.8 \cdot V_{OH}(DC)$.
- 3 Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching

Table 13 - LPDDR4X Differential Output Slew Rate for 0.6V VDDQ

Parameter	Symbol	Value		Unit
		Min	Max	
Differential Output Slew Rate ($V_{OH} = V_{DDQ} \cdot 0.5$)	SR_{Qdiff}^a	6	18	V/ns
^a SR: Slew Rate, Q: Query Output (like in DQ, which stands for Data-in, Query-Output), diff: differential Signals				

Note:

- 1 Measured with output reference load.
- 2 The output slew rate for falling and rising edges is defined and measured between $V_{OL}(AC) = -0.8 \cdot V_{OH}(DC)$ And $V_{OH}(AC) = 0.8 \cdot V_{OH}(DC)$.
- 3 Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

5 AC and DC Input/Output Measurement Levels

This chapter mainly defines DC electrical characteristics for input signals, AC overshoot and undershoot specifications, differential input voltage specifications, and output driver to ensure the normal operation of LPDDR4X SDRAM.

5.1 1.1V High Speed LVCMOS (HS_LLVC MOS)

5.1.1 Standard Specifications

All voltages are referenced to ground except where noted.

5.1.2 DC Electrical Characteristics

5.1.2.1 Input Level for CKE

This definition applies to CKE_A/ CKE_B.

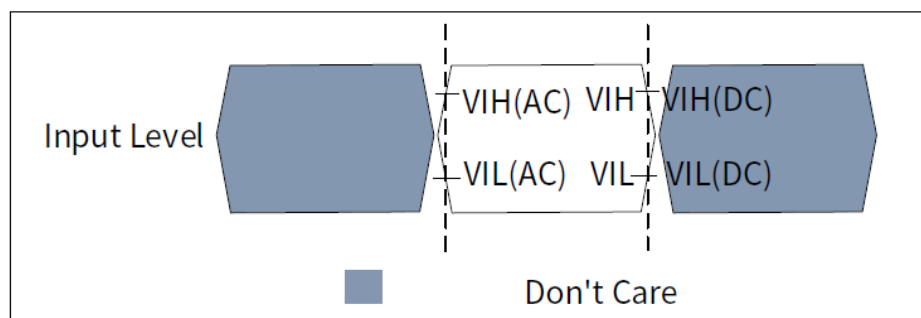
Table 14 - Input Level for CKE

Parameter	Symbol	Min	Max	Unit
Input high level (AC) ¹	VIH(AC)	0.75*VDD2	VDD2+0.2	V
Input low level (AC) ¹	VIL(AC)	-0.2	0.25*VDD2	V
Input high level (DC)	VIH(DC)	0.65*VDD2	VDD2+0.2	V
Input low level (DC)	VIL(DC)	-0.2	0.35*VDD2	V

Note:

Refer AC Overshoot and Undershoot for VIH(AC) and VIL(AC)

Figure 6 - Input AC Timing Definition for CKE



Note:

- 1 AC level is guaranteed transition point.
- 2 DC level is hysteresis.

5.1.2.2 Input Level for Reset_n and ODT_CA

This definition applies to Reset_n and ODT_CA.

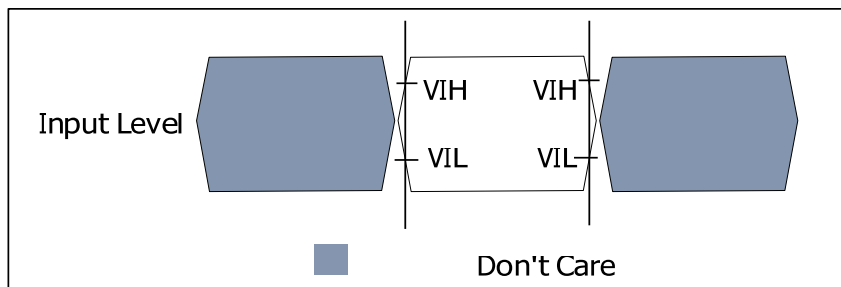
Table 15 - Input Level for Reset_n and ODT_CA

Parameter	Symbol	Min	Max	Unit
Input high level ¹	VIH	0.80*VDD2	VDD2+0.2	V
Input low level ¹	VIL	-0.2	0.20*VDD2	V

Note:

Refer AC Overshoot and Undershoot for VIH and VIL

Figure 7 - Input AC Timing Definition for Reset_n and ODT_CA

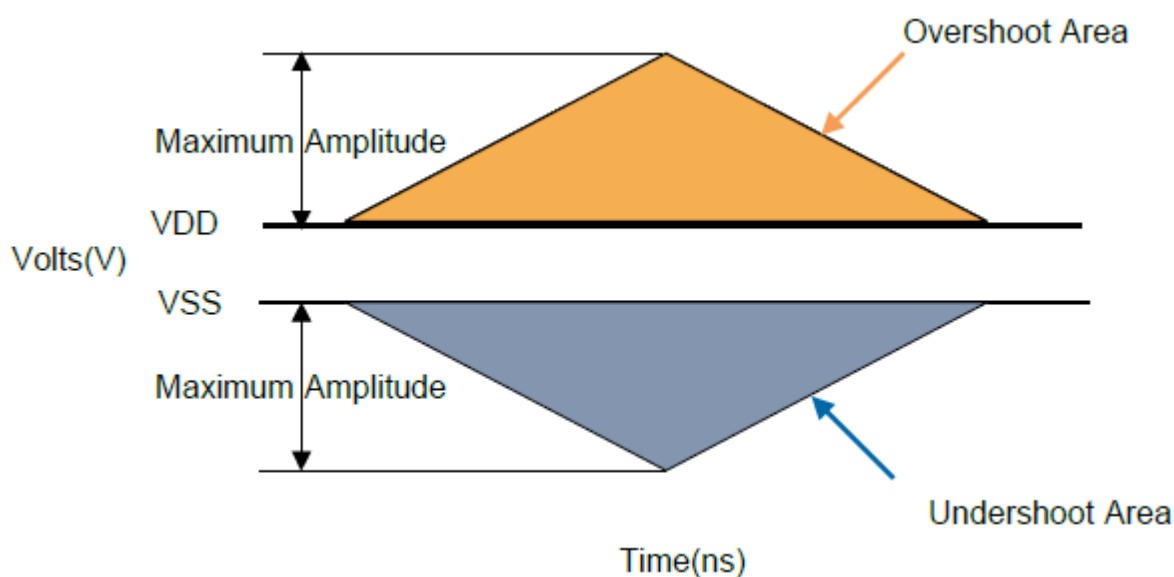


5.1.3 AC Overshoot and Undershoot

Table 16 - AC Over/Undershoot for Address and Control Pins

Parameter	Specification
Maximum peak Amplitude allowed for overshoot area	0.35 V
Maximum peak Amplitude allowed for undershoot area	0.35 V
Maximum overshoot area above VDD/VDDQ	0.8 V-ns
Maximum undershoot area below VSS/VSSQ	0.8 V-ns

Figure 8 - AC Overshoot and Undershoot Definition for Address and Control Pins



5.2 Differential Input Voltage

5.2.1 Differential Input Voltage for Clock

The minimum input voltage need to satisfy both Vindiff_CK and Vindiff_CK/2 specification at input receiver and their measurement period is 1tCK. Vindiff_CK is the peak to peak voltage centered on 0 volts differential and Vindiff_CK/2 is max and min peak voltage from 0V.

Figure 9 - CK Differential Input Voltage

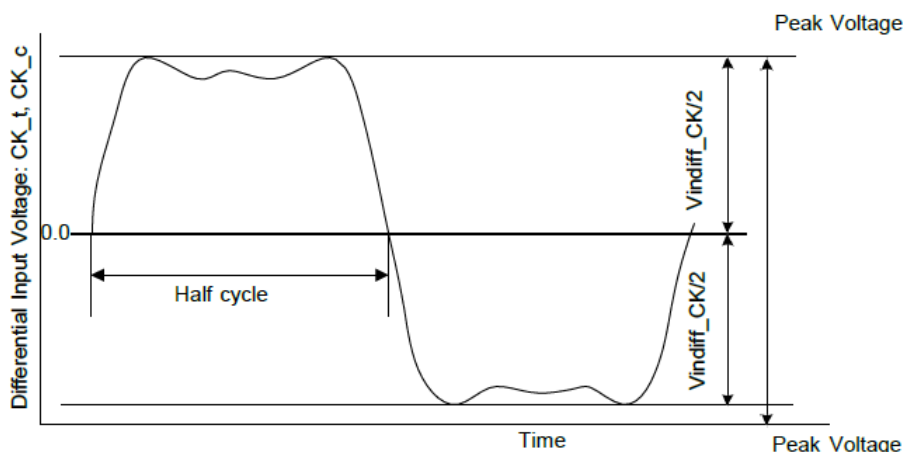


Table 17 - CK Differential Input Voltage

Parameter	Symbol	Data Rate						Unit
		1600/1867 ^a		2133/2400/3200		3733/4266		
		Min	Max	Min	Max	Min	Max	
CK differential input voltage	Vindiff_CK	420	-	380	-	360	-	mV
a. The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1867.								

Note:

The peak voltage of Differential CK signals is calculated in a following equation.

- $V_{indiff_CK} = (\text{Max Peak Voltage}) - (\text{Min Peak Voltage})$
- $\text{Max Peak Voltage} = \text{Max}(f(t))$
- $\text{Min Peak Voltage} = \text{Min}(f(t))$
- $f(t) = V_{CK_t} - V_{CK_c}$

5.2.2 Peak Voltage Calculation Method

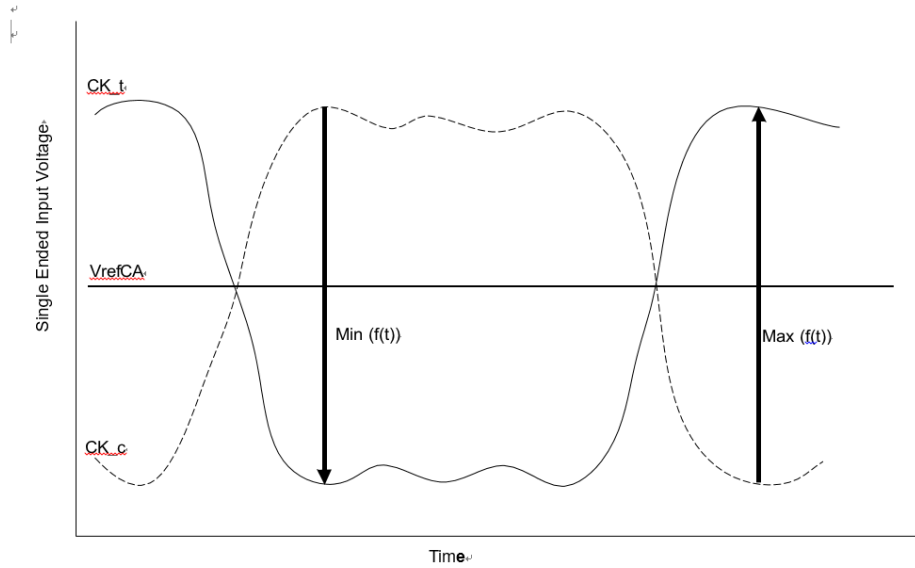
The peak voltage of Differential Clock signals are calculated in a following equation.

$$V_{IH.DIFF.PEAK} = \text{Max}(f(t))$$

$$V_{IL.DIFF.PEAK} = \text{Min}(f(t))$$

$$f(t) = V_{CK_t} - V_{CK_c}$$

Figure 10 - Definition of Differential Clock Peak Voltage



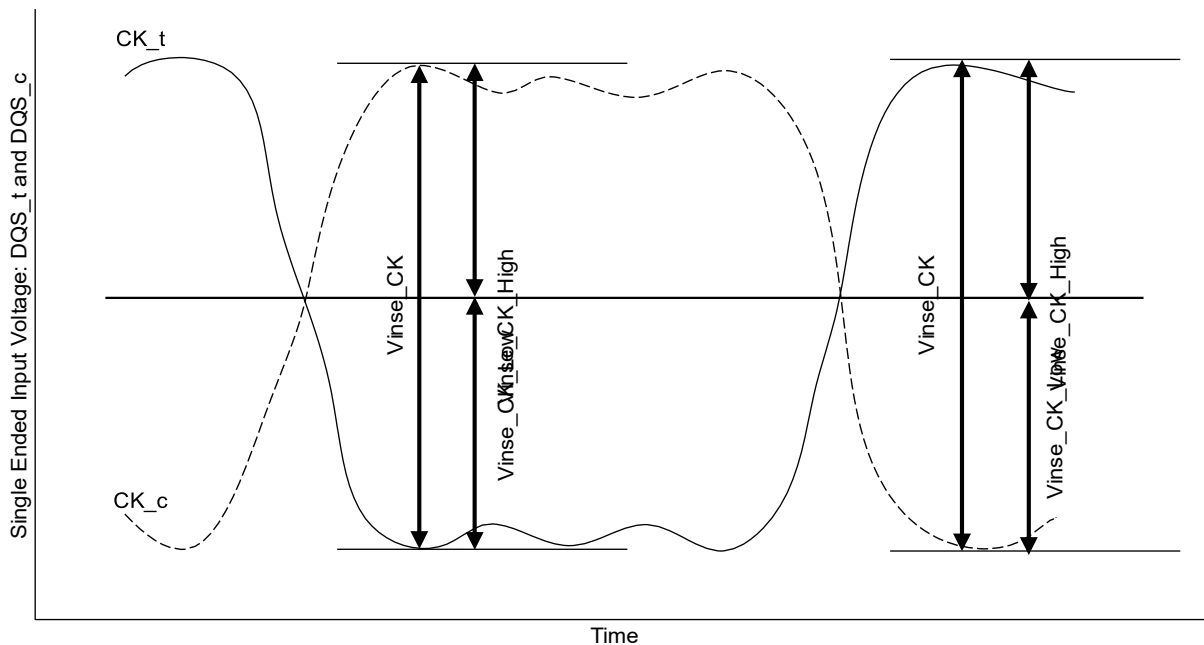
Note:

VREFCA is LPDDR4X SDRAM internal setting value by VREF Training.

5.3 Single-Ended Input Voltage for Clock

The minimum input voltage need to satisfy both V_{inse_CK} , $V_{inse_CK_High/Low}$ specification at input receiver.

Figure 11 - Clock Single-Ended Input Voltage



Note:

VREFCA is LPDDR4X SDRAM internal setting value by VREF Training.

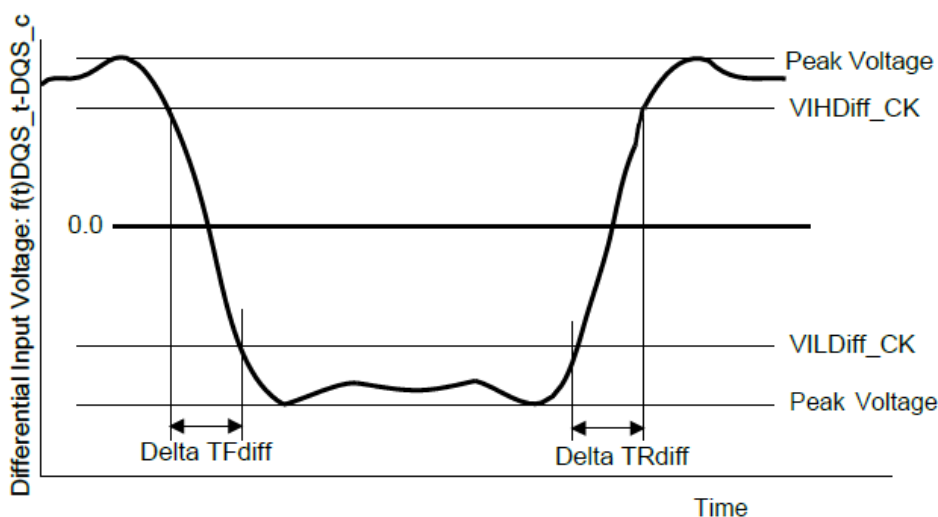
Table 18 - Clock Single-Ended Input Voltage

Parameter	Symbol	Data Rate						Unit
		1600/1867 ^a		2133/2400/3200		3733/4266		
		Min	Max	Min	Max	Min	Max	
Clock Single-Ended input voltage	Vinse_CK	210	-	190	-	180	-	mV
Clock Single-Ended input voltage High from VREFDQ	Vinse_CK_High	105	-	95	-	90	-	mV
Clock Single-Ended input voltage Low from VREFDQ	Vinse_CK_Low	105	-	95	-	90	-	mV
a. The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1867.								

5.3.1.1 Differential Input Slew Rate Definition for Clock

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown in Figure 15 and the following Tables.

Figure 12 - Differential Input Slew Rate Definition for CK_t, CK_c



Note:

- 1 Differential signal rising edge from VILdiff_CK to VIHdiff_CK must be monotonic slope.
- 2 Differential signal falling edge from VIHdiff_CK to VILdiff_CK must be monotonic slope.

Table 19 - Differential Input Slew Rate Definition for CK_t, CK_c

Description	From	To	Defined by
Differential input slew rate for rising edge(CK _t - CK _c)	VILdiff_CK	VIHdiff_CK	$ VILdiff_CK - VIHdiff_CK /DeltaTRdiff$
Differential input slew rate for falling edge(CK _t - CK _c)	VIHdiff_CK	VILdiff_CK	$ VILdiff_CK - VIHdiff_CK /DeltaTFdiff$

Table 20 - Differential Input Level for CK_t, CK_c

Parameter	Symbol	Data Rate						Unit
		1600/1867 ^a		2133/2400/3200		3733/4266		
		Min	Max	Min	Max	Min	Max	
Differential Input High	VIHdiff_CK	175	-	155	-	145	-	mV
Differential Input Low	VILdiff_CK	-	-175	-	-155	-	-145	mV
a. The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1867.								

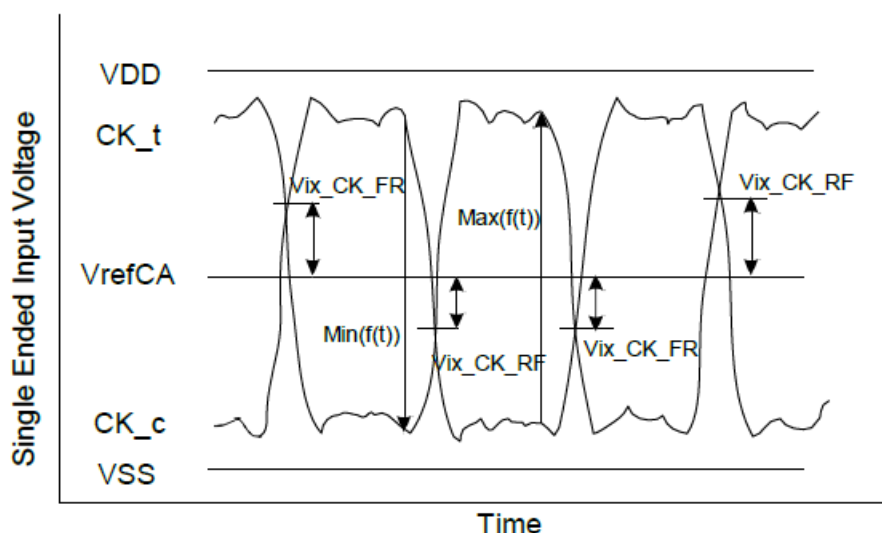
Table 21 - Differential Input Slew Rate for CK_t, CK_c

Parameter	Symbol	Data Rate						Unit
		1600/1867 ^a		2133/2400/3200		3733/4266		
		Min	Max	Min	Max	Min	Max	
Differential Input Slew Rate for Clock	SRIdiff_CK	2	14	2	14	2	14	V/ns
a. The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1867.								

5.3.1.2 Differential Input Cross Point Voltage

The cross point voltage of differential input signals (CK_t, CK_c) must meet the requirements in Table 22. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the mid level that is VREFCA.

Figure 13 - Vix Definition (Clock)



Note:

The base level of Vix_CK_FR/RF is VREFCA that is LPDDR4X SDRAM internal setting value by VREF Training.

Table 22 - Cross Point Voltage for Differential Input Signals (Clock)

Parameter	Symbol	Data Rate						Unit
		1600/1867 ^a		2133/2400/3200		3733/4266		
		Min	Max	Min	Max	Min	Max	
Clock Differential input cross point voltage ratio ^{1,2}	Vix_CK_ratio	-	25	-	25	-	25	%

a. The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1867.

Note:

- 1 Vix_CK_Ratio is defined by this equation: $Vix_CK_Ratio = Vix_CK_FR / |\text{Min}(f(t))|$
- 2 Vix_CK_Ratio is defined by this equation: $Vix_CK_Ratio = Vix_CK_RF / \text{Max}(f(t))$

5.3.1.3 Differential Input Voltage for DQS

The minimum input voltage need to satisfy both Vindiff_DQS and Vindiff_DQS/2 specification at input receiver and their measurement period is 1UI(tCK/2). Vindiff_DQS is the peak to peak voltage centered on 0 volts differential and Vindiff_DQS /2 is max and min peak voltage from 0V.

Figure 14 - DQS Differential Input Voltage

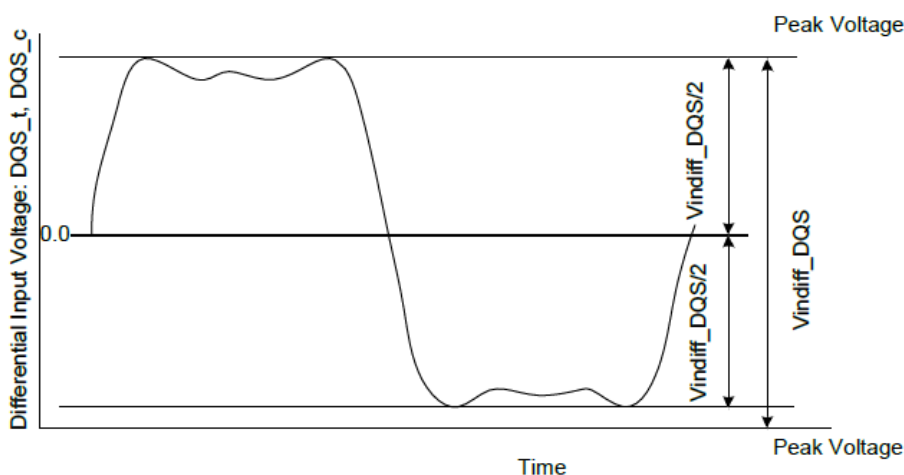


Table 23 - DQS Differential Input Voltage

Parameter	Symbol	Data Rate						Unit
		1600/1867 ^a		2133/2400/3200		3733/4266		
		Min	Max	Min	Max	Min	Max	
DQS differential input ¹	Vindiff_DQS	360	-	360	-	340	-	mV
a. The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1867.								

Note:

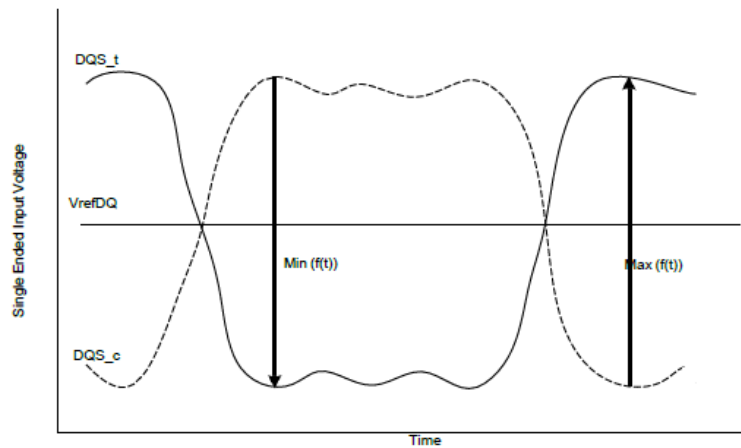
- 1 The peak voltage of Differential DQS signals is calculated in a following equation.
 - $Vindiff_DQS = (\text{Max Peak Voltage}) - (\text{Min Peak Voltage})$
 - $\text{Max Peak Voltage} = \text{Max}(f(t))$
 - $\text{Min Peak Voltage} = \text{Min}(f(t))$
 - $f(t) = VDQS_t - VDQS_c$

5.3.1.4 Peak Voltage Calculation Method

The peak voltage of Differential DQS signals are calculated in a following equation.

- $VIH.DIFF.\text{Peak Voltage} = \text{Max}(f(t))$
- $VIL.DIFF.\text{Peak Voltage} = \text{Min}(f(t))$
- $f(t) = VDQS_t - VDQS_c$

Figure 15 - Definition of Differential DQS Peak Voltage



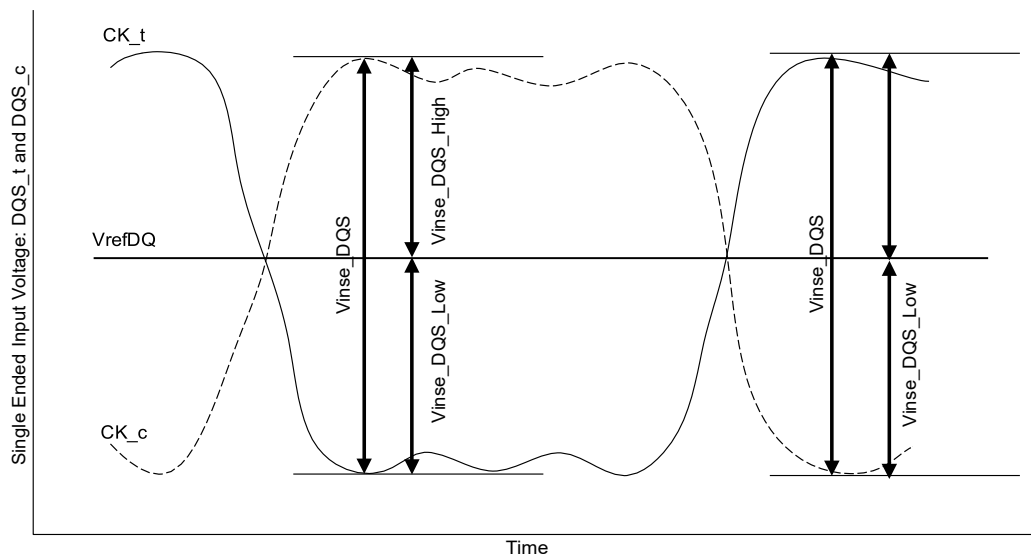
Note:

VrefDQ is LPDDR4X SDRAM internal setting value by Vref Training.

5.3.1.5 Single-Ended Input Voltage for DQS

The minimum input voltage need to satisfy both Vinse_DQS, Vinse_DQS_High/Low specification at input receiver.

Figure 16 - DQS Single-Ended Input Voltage



Note:

VrefDQ is LPDDR4X SDRAM internal setting value by Vref Training.

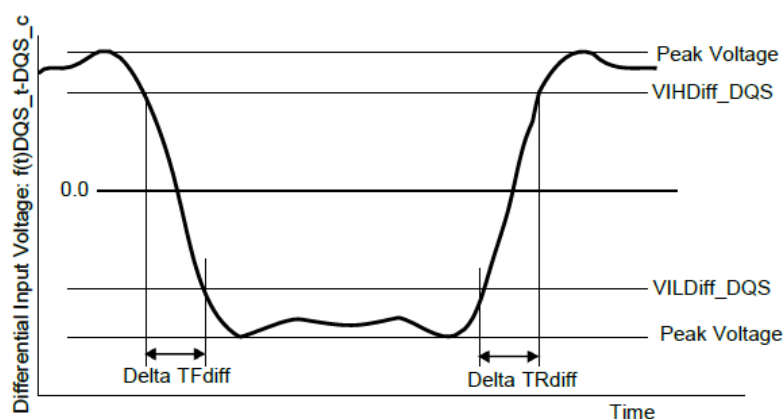
Table 24 - DQS Single-Ended Input Voltage

Parameter	Symbol	Data Rate						Unit
		1600/1867 ^a		2133/2400/3200		3733/4266		
		Min	Max	Min	Max	Min	Max	
DQS differential input	Vindiff_DQS	180	-	180	-	170	-	mV
DQS Single-Ended input voltage High from VREFDQ	Vinse_DQS_High	90	-	90	-	85	-	mV
DQS Single-Ended input voltage Low from VREFDQ	Vinse_DQS_Low	90	-	90	-	85	-	mV
a. The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1867.								

5.3.1.6 Differential Input Slew Rate Definition for DQS

Input slew rate for differential signals (DQS_t, DQS_c) are defined and measured as shown in Figure 17 and Table 25

Figure 17 - Differential Input Slew Rate Definition for DQS_t, DQS_c



Note:

- 1 Differential signal rising edge from VILdiff_DQS to VIHdiff_DQS must be monotonic slope.
- 2 Differential signal falling edge from VIHdiff_DQS to VILdiff_DQS must be monotonic slope.

Table 25 - Differential Input Slew Rate Definition for DQS_t, DQS_c

Description	From	To	Defined by
Differential input slew rate for rising edge(DQS _t - DQS _c)	VIHdiff_DQS	VIHdiff_DQS	$ VILdiff_DQS - VIHdiff_DQS /\Delta TRdiff$
Differential input slew rate for falling edge(DQS _t - DQS _c)	VIHdiff_DQS	VIHdiff_DQS	$ VILdiff_DQS - VIHdiff_DQS /\Delta TFdiff$

Table 26 - Differential Input Level for DQS_t, DQS_c

Parameter	Symbol	Data Rate						Unit
		1600/1867 ^a		2133/2400/3200		3733/4266		
		Min	Max	Min	Max	Min	Max	
Differential Input High	VIHdiff_DQS	140	-	140	-	120	-	mV
Differential Input Low	VILdiff_DQS	-	-140	-	-140	-	-120	mV
a. The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1867.								

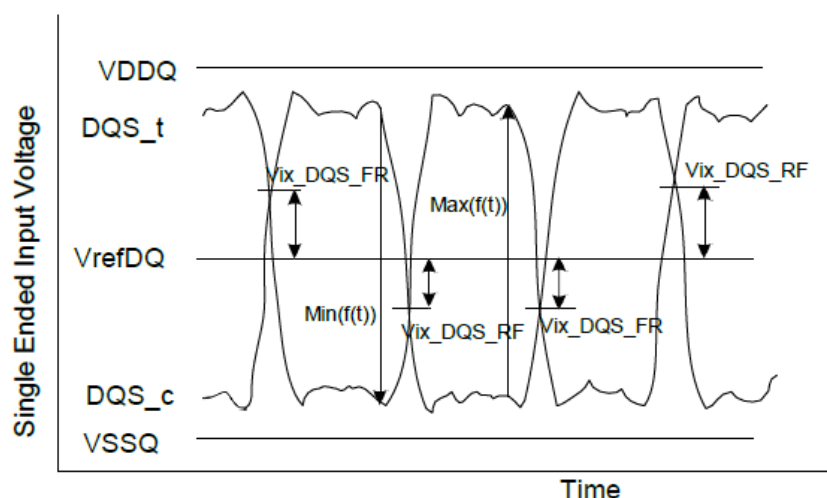
Table 27 - Differential Input Slew Rate for DQS_t, DQS_c

Parameter	Symbol	Data Rate						Unit
		1600/1867 ^a		2133/2400/3200		3733/4266		
		Min	Max	Min	Max	Min	Max	
Differential Input Slew Rate	SRIdiff	2	14	2	14	2	14	V/ns

5.3.1.7 Differential Input Cross Point Voltage

The cross point voltage of differential input signals (DQS_t, DQS_c) must meet the requirements in Table 28. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the mid level that is VREFDQ.

Figure 18 - Vix Definition (DQS)



Note:

The base level of Vix_DQS_FR/RF is VrefDQ that is LPDDR4X SDRAM internal setting value by Vref Training.

Table 28 - Cross Point Voltage for Differential Input Signals(DQS)

Parameter	Symbol	Data Rate						Unit
		1600/1867 ^a		2133/2400/3200		3733/4266		
		Min	Max	Min	Max	Min	Max	
DQS Differential input cross point voltage ratio ^{1,2}	Vix_DQS_ratio	-	20	-	20	-	20	%
a.The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1867.								

Note:

- Vix_DQS_Ratio is defined by this equation: $Vix_DQS_Ratio = Vix_DQS_FR / |Min(f(t))|$.
- Vix_DQS_Ratio is defined by this equation: $Vix_DQS_Ratio = Vix_DQS_RF / Max(f(t))$.

5.4 AC/DC Input level for ODT Input

Table 29 - Input Level for ODT

Parameter	Symbol	Min	Max	Unit
ODT Input High Level (AC) ¹	VIHODT(AC)	0.75*VDD	VDD+0.2	V
ODT Input Low Level (AC) ¹	VILODT(AC)	-0.2	0.25*VDD	V
ODT Input High Level (DC)	VIHODT(DC)	0.65*VDD	VDD+0.2	V

ODT Input Low Level (DC)	VILODT(DC)	-0.2	0.35*VDD	V
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Note:

See Overshoot and Undershoot Specifications

5.5 Overshoot and Undershoot for LVSTL

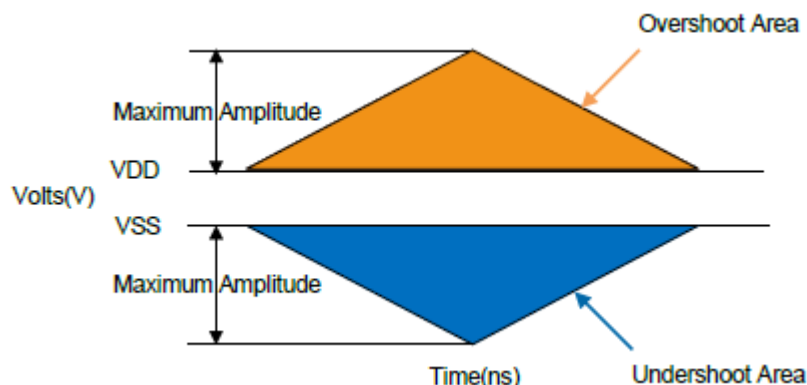
Table 30 - AC Overshoot/Undershoot Specification

Parameter	Min/Max	Data Rate		Unit
		1600/1866/3200	4266	
Maximum peak amplitude allowed for overshoot area. See Figure 19	Max	0.3	t.b.d	V
Maximum peak amplitude allowed for undershoot area. See Figure 19	Max	0.3	t.b.d	V
Maximum area above VDD /VDDQ. See Figure 19	Max	0.1	t.b.d	V/ns
Maximum area below VSS. See Figure 19	Max	0.1	t.b.d	V/ns

Note:

- 1 VDD2 stands for VDD for CA[5:0], CK_t, CK_c, CS_n, CKE and ODT. VDD stands for VDDQ for DQ, DMI, DQS_t and DQS_c.
- 2 VSS stands for VSS for CA[5:0], CK_t, CK_c, CS_n, CKE and ODT. VSS stands for VSSQ for DQ, DMI, DQS_t and DQS_c.
- 3 Maximum peak amplitude values are referenced from actual VDD and VSS values.
- 4 Maximum area values are referenced from maximum operating VDD and VSS values.

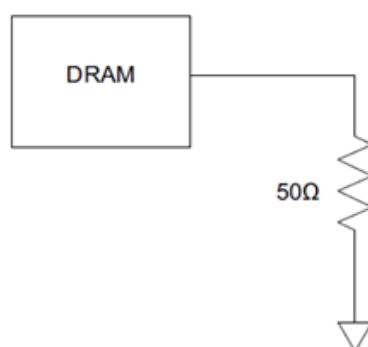
Figure 19 - Overshoot and Undershoot Definition



5.6 Driver Output Timing Reference Load

These 'Timing Reference Loads' are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

Figure 20 - Driver Output Reference Load for Timing and Slew Rate



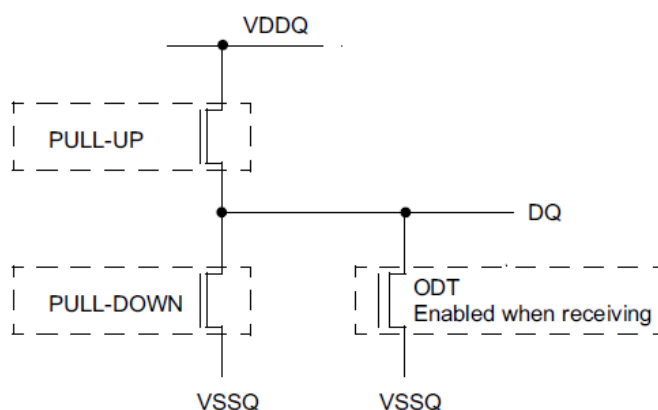
Note:

All output timing parameter values are reported with respect to this reference load. This reference load is also used to report slew rate.

5.7 LVSTL(Low Voltage Swing Terminated Logic) IO System

LVSTL I/O cell is comprised of pull-up, pull-down driver and a terminator. The basic cell is shown in Figure 21.

Figure 21 - LVSTL I/O Cell

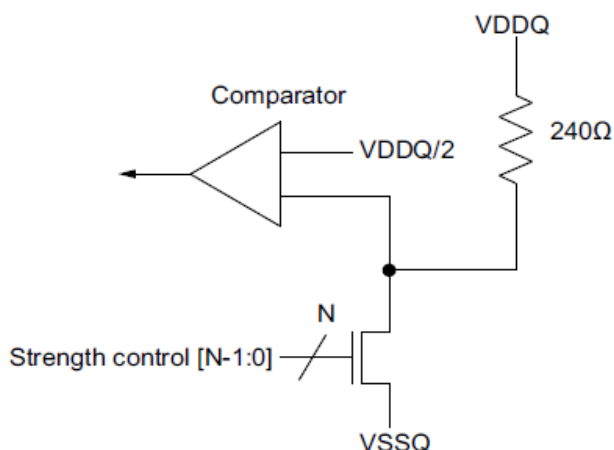


To ensure that the target impedance is achieved the LVSTL I/O cell is designed to be calibrated as below procedure.

First calibrate the pull-down device against a 240 Ω resistor to VDDQ via the ZQ pin.

- Set Strength Control to minimum setting.
- Increase drive strength until comparator detects data bit is less than $VDDQ/2$.
- NMOS pull-down device is calibrated to 240 Ω.

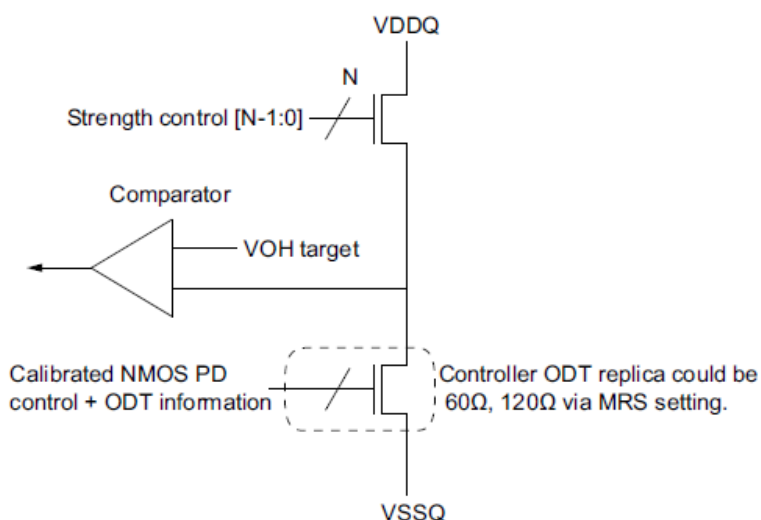
Figure 22 - Pull-down Calibration



Then calibrate the pull-up device against the calibrated pull-down device.

- Set VOH target and NMOS controller ODT replica via MRS (VOH can be automatically controlled by ODT MRS).
- Set Strength Control to minimum setting.
- Increase drive strength until comparator detects data bit is greater than VOH target.
- NMOS pull-up device is now calibrated to VOH target.

Figure 23 - Pull-up Calibration



6 Input/Output Capacitance

Table 31 - Input/output Capacitance

Parameter	Symbol	Min/Max	3200 - 533	3733/4266	Unit	Note
Input capacitance, CK_t and CK_c	C _{CK}	Min	0.5	TBD	pF	1,2
		Max	0.9	TBD		
Input capacitance delta, CK_t and CK_c	C _{DCK}	Min	0.0	TBD	pF	1,2,3
		Max	0.09	TBD		
Input capacitance, all other input-only pins	C _I	Min	0.5	TBD	pF	1,2,4
		Max	0.9	TBD		
Input capacitance delta, all other input-only pins	C _{DI}	Min	-0.1	TBD	pF	1,2,5
		Max	0.1	TBD		
Input/output capacitance, DQ, DMI, DQS_t, DQS_c	C _{IO}	Min	0.7	TBD	pF	1,2,6
		Max	1.3	TBD		
Input/output capacitance delta, DQS_t, DQS_c	C _{DDQS}	Min	0.0	TBD	pF	1,2,7
		Max	0.1	TBD		
Input/output capacitance delta, DQ, DMI	C _{DIO}	Min	-0.1	TBD	pF	1,2,8
		Max	0.1	TBD		
Input/output capacitance, ZQ pin	C _{ZQ}	Min	0.0	TBD	pF	1,2
		Max	5.0	TBD		

Note:

- 1 This parameter applies to die device only (does not include package capacitance).
- 2 This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSQ applied and all other pins floating.
- 3 Absolute value of CCK_t . CCK_c.
- 4 CI applies to CS_n, CKE, CA0~CA5.
- 5 CDI = CI . 0.5 * (CCK_t + CCK_c).
- 6 DMI loading matches DQ and DQS.
- 7 Absolute value of CDQS_t and CDQS_c.
- 8 CDIO = CIO . 0.5 * (CDQS_t + CDQS_c) in byte-lane.

7 IDD Test Conditions and Specifications

In this chapter, IDD measurement conditions including CA patterns and DQ patterns are defined.
The key performance indicator IDD values are introduced in the second section of this chapter.

7.1 IDD Measurement Conditions

The following definitions are used within the IDD measurement tables unless stated otherwise: LOW: $V_{IN} \leq V_{IL}(DC)_{MAX}$
HIGH: $V_{IN} \geq V_{IH}(DC)_{MIN}$

STABLE: Inputs are stable at a HIGH or LOW level SWITCHING: See Table 32 and Table 33.

Table 32 - Definition of Switching for CA Input Signals

Switching for CA								
CK_t Edge	R1	R2	R3	R4	R5	R6	R7	R8
CKE	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
CS	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

Note:

- 1 CS must always be driven LOW.
- 2 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.
- 3 The pattern is used continuously during IDD measurement for IDD values that require switching on the CA bus.

Table 33 - CA Pattern for IDD4R

Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	HIGH	Read-1	L	L	L	L	L	L
N+9	HIGH	LOW		L	L	L	L	L	L
N+10	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+11	HIGH	LOW		H	H	H	H	H	H
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L

Note:

- 1 BA[2:0] = 010, CA[9:4] = 000000 or 111111, Burst Order CA[3:2] = 00 or 11 (Same as LPDDR3 IDD4R).
- 2 Difference from LPDDR3 (JESD209-3): CA pins are kept low with DES CMD to reduce ODT current.

Table 34 - CA Pattern for IDD4Wc

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+9	HIGH	LOW		L	H	L	L	H	L
N+10	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+11	HIGH	LOW		L	L	H	H	H	H
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L

Note:

- 1 BA[2:0] = 010, CA[9:4] = 000000 or 111111 (Same as LPDDR3 IDD4W).
- 2 Difference from LPDDR3 (JESD209-3): 1)-No burst ordering, and 2) CA pins are kept low with DES CMD to reduce ODT current.

Table 35 - Data Pattern for IDD4W (DBI off)

DBI OFF Case										No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	0	0	0	6
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	1	1	1	1	1	1	1	1	0	8
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	0	0	0	6
BL27	1	1	1	1	0	0	0	0	0	4
BL28	1	1	1	1	1	1	1	1	0	8
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
No. of 1's	16	16	16	16	16	16	16	16		

Note:

Simplified pattern compared predecessor. Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

Table 36 - Data Pattern for IDD4R (DBI off)

DBI OFF Case										No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	1	1	0	8
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	1	1	1	1	1	1	0	0	0	6
BL21	1	1	1	1	0	0	0	0	0	4
BL22	0	0	0	0	0	0	1	1	0	2
BL23	0	0	0	0	1	1	1	1	0	4
BL24	0	0	0	0	0	0	1	1	0	0
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	1	1	0	8
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	1	1	0	2
BL29	0	0	0	0	1	1	1	1	0	4
BL30	1	1	1	1	1	1	0	0	0	6
BL31	1	1	1	1	0	0	0	0	0	4
No. of 1's	16	16	16	16	16	16	16	16	16	

Note:

Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming

Table 37 - Data Pattern for IDD4W (DBI On)

DBI ON Case										No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	0	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	0	0	0	1
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	1	1	1	3
BL21	0	0	0	0	1	1	1	1	0	4
BL22	0	0	0	0	0	0	1	1	0	2
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	0	0	0	1
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	1	1	0	2
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	1	1	1	3
BL31	0	0	0	0	1	1	1	1	0	4
No. of 1's	8	8	8	8	8	8	16	16	8	

Note:

DBI enabled burst

Table 38 - Data Pattern for IDD4R (DBI On)

DBI ON Case										No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	0	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	0	0	0	1
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	1	1	1	3
BL21	0	0	0	0	1	1	1	1	0	4
BL22	0	0	0	0	0	0	1	1	0	2
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	0	0	0	1
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	1	1	0	2
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	1	1	1	3
BL31	0	0	0	0	1	1	1	1	0	4
No. of 1's	8	8	8	8	8	8	16	16	8	

7.2 IDD Specifications

IDD values are for the entire operating voltage range, and all of them are for the entire standard range, with the exception

of IDD6ET which is for the entire elevated temperature range.

Table 39 - IDD Specification Parameters and Operating Conditions

Parameter/Condition	Symbol	Power Supply	Note
Operating one bank active-precharge current: tCK = tCKmin; tRC = tRCmin; CKE is HIGH; CS is LOW between valid commands; CA bus inputs are switching; Data bus inputs are stable, ODT disabled	IDD01	VDD1	
	IDD02	VDD2	
	IDD0Q	VDDQ	3
Idle power-down standby current: tCK = tCKmin; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable, ODT disabled	IDD2P1	VDD1	
	IDD2P2	VDD2	
	IDD2PQ	VDDQ	3
Idle power-down standby current with clock stop: CK_t = LOW, CK_c = HIGH; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable, ODT disabled	IDD2PS1	VDD1	
	IDD2PS2	VDD2	
	IDD2PSQ	VDDQ	3
Idle non power-down standby current: tCK = tCKmin; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable, ODT disabled	IDD2N1	VDD1	
	IDD2N2	VDD2	
	IDD2NQ	VDDQ	3
Idle non power-down standby current with clock stopped: CK_t = LOW; CK_c = HIGH; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable, ODT disabled	IDD2NS1	VDD1	
	IDD2NS2	VDD2	
	IDD2NSQ	VDDQ	3
Active power-down standby current: tCK = tCKmin; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable, ODT disabled	IDD3P1	VDD1	
	IDD3P2	VDD2	
	IDD3PQ	VDDQ	3
Active power-down standby current with clock stop: CK_t = LOW, CK_c = HIGH; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable, ODT disabled	IDD3PS1	VDD1	
	IDD3PS2	VDD2	
	IDD3PSQ	VDDQ	4
Active non-power-down standby current: tCK = tCKmin; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable, ODT disabled	IDD3N1	VDD1	
	IDD3N2	VDD2	
	IDD3NQ	VDDQ	4
Active non-power-down standby current with clock stopped: CK_t = LOW, CK_c = HIGH; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable, ODT disabled	IDD3NS1	VDD1	
	IDD3NS2	VDD2	
	IDD3NSQ	VDDQ	4
Operating burst READ current: tCK = tCKmin; CS is LOW between valid commands; One bank is active; BL = 16 or 32; RL = RL(MIN); CA bus inputs are switching; 50% data change each burst transfer ODT disabled	IDD4R1	VDD1	
	IDD4R2	VDD2	
	IDD4RQ	VDDQ	5
Operating burst WRITE current: tCK = tCKmin; CS is LOW between valid commands; One bank is active; BL = 16 or 32; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer ODT disabled	IDD4W1	VDD1	
	IDD4W2	VDD2	
	IDD4WQ	VDDQ	4
All bank REFRESH Burst current: tCK = tCKmin; CKE is HIGH between valid commands; tRC = tRFCabmin; Burst refresh; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	IDD51	VDD1	
	IDD52	VDD2	
	IDD5Q	VDDQ	4

Parameter/Condition	Symbol	Power Supply	Note
All bank REFRESH Average current:tCK = tCKmin;CKE is HIGH between valid commands;tRC = tREFI;CA bus inputs are switching;Data bus inputs are stable;ODT disabled Per bank REFRESH Average current:tCK = tCKmin; CKE is HIGH between valid commands;tRC = tREFI/8;CA bus inputs are switching;Data bus inputs are stable;ODT disabled	IDD5AB1	VDD1	
	IDD5AB2	VDD2	
	IDD5ABQ	VDDQ	4
	IDD5PB1	VDD1	
	IDD5PB2	VDD2	
	IDD5PBQ	VDDQ	4
Power Down Self Refresh current (-25 ° C to +85 ° C):CK_t=LOW, CK_c=HIGH;CKE is LOW;CA bus inputs are stable;Data bus inputs are stable;Maximum 1x Self Refresh Rate;ODT disabled	IDD61	VDD1	6,7,8,10
	IDD62	VDD2	6,7,8,10
	IDD6Q	VDDQ	4,6,7,8,10
Power Down Self Refresh current (+85 ° C to +105 ° C): CK_t=LOW, CK_c=HIGH;CKE is LOW;CA bus inputs are stable;Data bus inputs are stable;Maximum 1x Self Refresh Rate;ODT disabled	IDD6ET1	VDD1	7,8,11
	IDD6ET2	VDD2	7,8,11
	IDD6ETQ	VDDQ	4,7,8,11

Note:

- 1 DBI Published IDD values are the maximum of the distribution of the arithmetic mean.
- 2 ODT disabled: MR11[2:0] = 000B.
- 3 IDD current specifications are tested after the device is properly initialized.
- 4 Measured currents are the summation of VDDQ and VDD2.
- 5 Guaranteed by design with output load = 5pF and RON = 40 Ω.
- 6 The 1x Self Refresh Rate is the rate at which the LPDDR4 device is refreshed internally during Self Refresh, before going into the elevated Temperature range.
- 7 This is the general definition that applies to full array Self Refresh.
- 8 Supplier datasheets may contain additional Self Refresh IDD values for temperature subranges within the Standard or elevated Temperature Ranges.
- 9 For all IDD measurements, VIHCKE = 0.8 x VDD2, VILCKE = 0.2 x VDD2.
- 10 IDD6 85 °C is guaranteed, IDD6 45 °C is typical of the distribution of the arithmetic mean.
- 11 IDD6ET is a typical value, is sampled only, and is not tested.
- 12 Dual Channel devices are specified in dual channel operation (both channels operating together).

7.3 LPDDR4X IDD Parameters - Single Die

VDD2 = 1.06 ~ 1.17V, VDDQ = 0.57 ~ 0.65V; VDD1 = 1.70 ~ 1.95V; T_C = -25°C ~ +85°C

Symbol	Supply	4266 Mbps	Unit
IDD0 ₁	VDD1	2.85	mA
IDD0 ₂	VDD2	57.25	
IDD0Q	VDDQ	1.2	
IDD2P ₁	VDD1	0.56	mA
IDD2P ₂	VDD2	1.83	
IDD2PQ	VDDQ	1.2	
IDD2PS ₁	VDD1	0.56	mA
IDD2PS ₂	VDD2	1.82	
IDD2PSQ	VDDQ	1.2	
IDD2N ₁	VDD1	0.56	mA
IDD2N ₂	VDD2	32.62	

IDD2NQ	VDDQ	1.2	mA
IDD2NS ₁	VDD1	0.56	
IDD2NS ₂	VDD2	27.67	
IDD2NSQ	VDDQ	1.2	
IDD3P ₁	VDD1	0.58	mA
IDD3P ₂	VDD2	11.34	
IDD3PQ	VDDQ	1.2	
IDD3PS ₁	VDD1	0.58	mA
IDD3PS ₂	VDD2	11.34	
IDD3PSQ	VDDQ	1.2	
IDD3N ₁	VDD1	1.23	mA
IDD3N ₂	VDD2	41.31	
IDD3NQ	VDDQ	1.2	
IDD3NS ₁	VDD1	1.24	mA
IDD3NS ₂	VDD2	36.36	
IDD3NSQ	VDDQ	1.2	
IDD4R ₁	VDD1	3.56	mA
IDD4R ₂	VDD2	237.89	
IDD4RQ	VDDQ	67.49	
IDD4W ₁	VDD1	3.16	mA
IDD4W ₂	VDD2	189.99	
IDD4WQ	VDDQ	1.2	

Symbol	Supply	4266 Mbps	Unit
IDD5 ₁	VDD1	10.88	mA
IDD5 ₂	VDD2	117.18	
IDD5Q	VDDQ	1.2	
IDD5AB ₁	VDD1	1.38	mA
IDD5AB ₂	VDD2	36.89	
IDD5ABQ	VDDQ	1.2	
IDD5PB ₁	VDD1	1.42	mA
IDD5PB ₂	VDD2	37.48	
IDD5PBQ	VDDQ	1.2	

7.4 LPDDR4X IDD6 Parameters - Single Die

VDD2 = 1.06 ~ 1.17V, VDDQ = 0.57 ~ 0.65V; VDD1 = 1.70 ~ 1.95V; T_C = -25°C ~ +85°C

Temperature	Symbol	Supply	Full-Array Self Refresh Current	Unit	Note
25°C	IDD6 ₁	VDD1	0.42	mA	
	IDD6 ₂	VDD2	1.26		
	IDD6Q	VDDQ	1.2		

85°C	IDD6 ₁	VDD1	2.04	mA	
	IDD6 ₂	VDD2	15.85		
	IDD6Q	VDDQ	1.2		

8 Electrical Characteristics and AC Timing

8.1 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the LPDDR4X device.

8.1.1 Definition for tCK(avg) and nCK

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left[\sum_{j=1}^N tCK_j \right] / N \quad N=200$$

Unit 'tCK(avg)' represents the actual clock average tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges. tCK(avg) may change by up to +/-1% within a 100 clock cycle window, provided that all jitter and timing specs are met.

8.1.2 Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge.

tCK(abs) is not subject to production test.

8.1.2.1 Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left[\sum_{j=1}^N tCH_j \right] / \{N \times tCK(avg)\} \quad N=200$$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left[\sum_{j=1}^N tCL_j \right] / \{N \times tCK(avg)\} \quad N=200$$

8.1.2.2 Definition for tCH(abs) and tCL(abs)

tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.

tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.

Both tCH(abs) and tCL(abs) are not subject to production test.

8.1.2.3 Definition for tJIT(per)

tJIT(per) is the single period jitter defined as the largest deviation of any signal tCK from tCK(avg).

$tJIT(per) = \text{Min/max of } \{tCK_i - tCK(avg) \text{ where } i = 1 \text{ to } 200\}$.

tJIT(per),act is the actual clock jitter for a given system.

tJIT(per),allowed is the specified allowed clock period jitter.

tJIT(per) is not subject to production test.

8.1.2.4 Definition for tJIT(cc)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles.

$tJIT(cc) = \text{Max of } \{tCK(i+1) - tCK(i)\}$. tJIT(cc) defines the cycle to cycle jitter.

tJIT(cc) is not subject to production test.

8.2 Clock Timing

Table 40 - Clock AC Timings

Parameter	Symbol	1600/2400/3200				Unit
		Min		Max		
Clock Timing						
Average High pulse width	tCH(avg)	0.46		0.54		tCK(avg)
Average Low pulse width	tCL(avg)	0.46		0.54		tCK(avg)
Absolute clock period	tCK(abs)	tCK(avg)MIN +tJIT(per)MIN			-	ns
Absolute High clock pulse width	tCH(abs)	0.43		0.57		tCK(avg)
Absolute Low clock pulse width	tCL(abs)	0.43		0.57		tCK(avg)

Parameter	Symbol	1600		2400		3200		4266		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Clock Timing										
Average clock period	tCK(avg)	1.25	100	0.833	100	0.625	100	0.468	100	ns
Clock period jitter	tJIT(per)	-70	70	-50	50	-40	40	-	TBD	ps
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	140	-	100	-	80	-	TBD	ps

8.3 Temperature Derating for AC Timing

Table 41 - Temperature Derating AC Timing

Parameter	Symbol	Min/Max	Data Rate	Unit
			533/1066/1600/2133/ 2667/3200/3733/4267	
Temperature Derating ¹				

DQS output access time from CK_t/CK_c (derated)	tDQSCK	Min	3600	ps
RAS-to-CAS delay (derated)	tRCD	Min	tRCD + 1.875	ns

Parameter	Symbol	Min/Max	Data Rate	Unit
			533/1066/1600/2133/ 2667/3200/3733/4267	
ACTIVATE-to- ACTIVATE command period (derated)	tRC	Min	tRC + 3.75	ns
Row active time (derated)	tRAS	Min	tRAS + 1.875	ns
Row precharge time (derated)	tRP	Min	tRP + 1.875	ns
Active bank A to active bank B (derated)	tRRD	Min	tRRD + 1.875	ns

Note:

Timing derating applies for operation at 85 °C to 105 °C.

8.4 CA Rx Voltage and Timing

The command and address(CA) including CS input receiver compliance mask for voltage and timing is shown in Figure 24. All CA, CS signals apply the same compliance mask and operate in single data rate mode.

The CA input receiver mask for voltage and timing is shown in Figure 25. The receiver mask(Rx Mask) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal; it is not the valid data-eye.

Figure 24 - CA Receiver(Rx) Mask

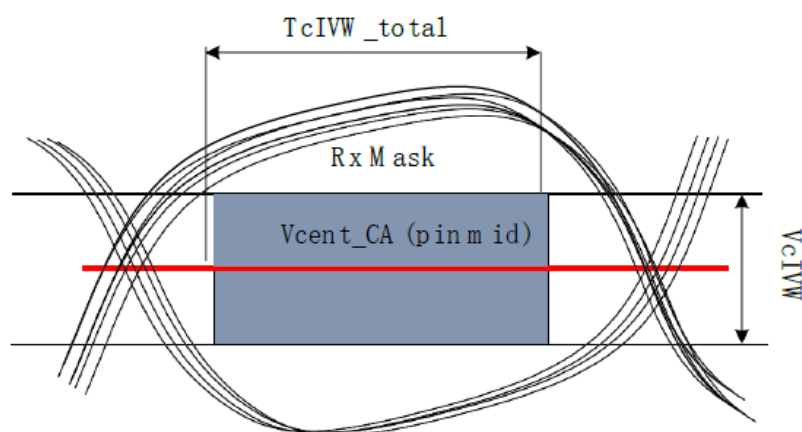
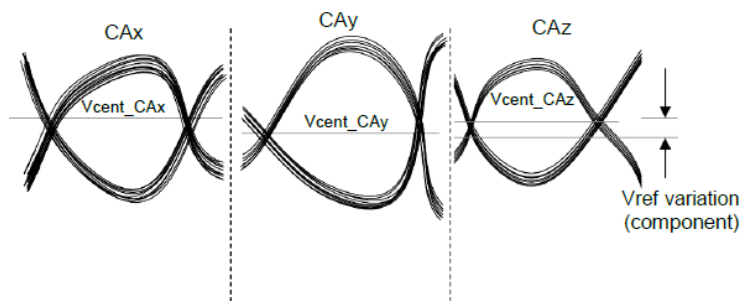


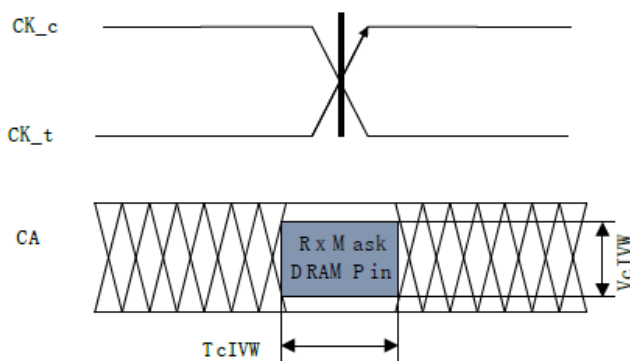
Figure 25 - Across Pin VREFCA Voltage Variation



Vcent_CA(pin mid) is defined as the midpoint between the largest Vcent_CA voltage level and the smallest Vcent_CA voltage level across all CA and CS pins for a given DRAM component. Each CA Vcent level is defined by the center, i.e., widest opening, of the cumulative data input eye as depicted in Figure 255. This clarifies that any DRAM component level variation must be accounted for within the DRAM CA Rx mask. The component level VREF will be set by the system to account for Ron and ODT settings.

Figure 26 - CA Timings at the DRAM Pins

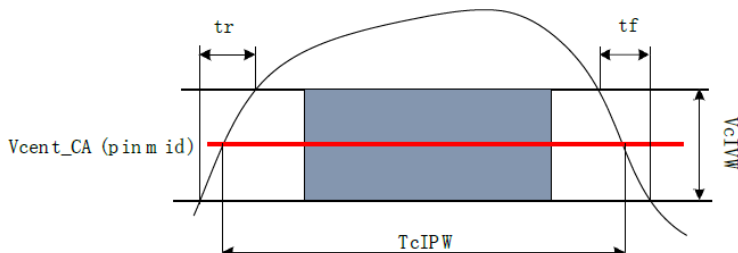
CK_t, CK_c Data-in at DRAM Ball Maximum CA Eye center aligned



TcIVW for all CA signals is defined as centered on the CK_t/CK_c crossing at DRAM pin

All of the timing terms in Figure 26 are measured from the CK_t/CK_c to the center(midpoint) of the TcIVW window taken at the VcIVW_total voltage levels centered around Vcent_CA(pin mid).

Figure 27 - CA TcIPW and SRIN_cIVW definition (for each input pulse)



Note:

SRIN_cIVW=VcIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.

Figure 28 - CA VIH_L_AC Definition (for Each Input Pulse)

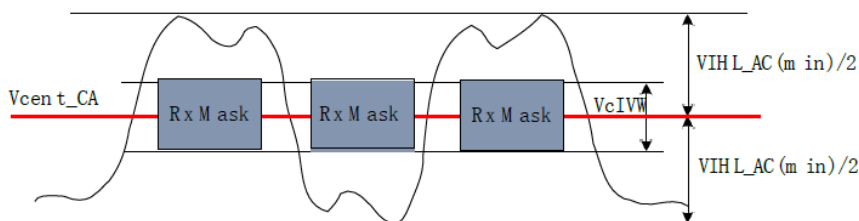


Table 42 - DRAM CMD/ADR, CS

* UI=tck(avg)min

Symbol	Parameter	DQ-1333 ^a /1600/186		DQ-3200		DQ-4266		Unit	Note
		Min	Max	Min	Max	Min	Max		
VcIVW	Rx Mask voltage - p-p	-	175	-	155	-	145	mV	1,2,3
TcIVW	Rx timing window	-	0.3	-	0.3	-	0.3	UI	
VIHL_AC	CAAC input pulse amplitude pk-	210	-	190	-	180	-	mV	4,7
TcIPW	CA input pulse width	0.55		0.6		0.6		UI	5
SRIN_cIV	Input Slew Rate over VcIVW	1	7	1	7	1	7	V/ns	6

a. The following Rx voltage and absolute timing requirements apply for DQ operating frequencies at or below

Note:

- 1 CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.

- 2 Rx mask voltage VclVW total(max) must be centered around Vcent_CA(pin mid).
- 3 Vcent_CA must be within the adjustment range of the CA internal Vref.
- 4 CA only input pulse signal amplitude into the receiver must meet or exceed VIH_{LAC} at any point over the total UI.
No timing requirement above level. VIH_{LAC} is the peak to peak voltage centered around Vcent_CA(pin mid) such that VIH_{LAC}/2 min must be met both above and below Vcent_CA.
- 5 CA only minimum input pulse width defined at the Vcent_CA(pin mid).
- 6 Input slew rate over VclVW Mask centered at Vcent_CA(pin mid).
- 7 VIH_{LAC} does not have to be met when no transitions are occurring.

8.5 DRAM Data Timing

Figure 29 - Read Data Timing Definitions t_{QH} and t_{DQSQ} across all DQ Signals per DQS Group

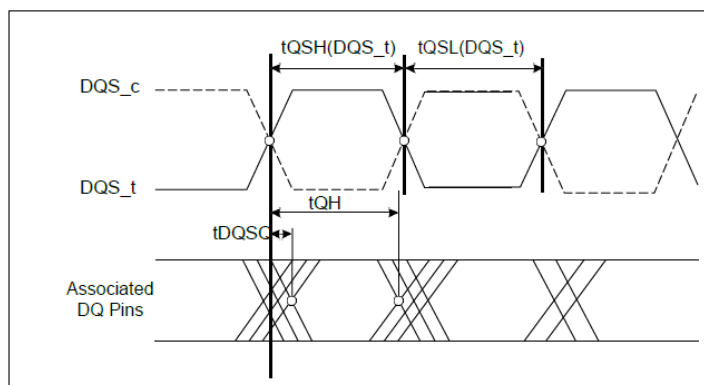


Figure 30 - Read Data Timing t_{QW} Valid Window Defined per DQ Signal

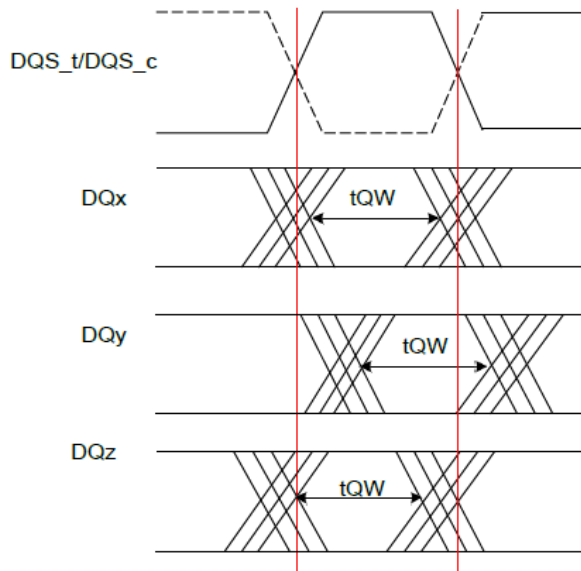


Table 43 - Read Output Timings

Unit UI = tCK(avg)min/2

Symbol	Parameter	DQ-1600/1867		DQ-2133/2400		DQ-3200		DQ-4266		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data Timing											
tDQSQ	DQS_t,DQS_c to DQ Skew total, per group, per access (DBI Disabled)	-	0.18	-	0.18	-	0.18	-	0.18	UI	

tQH	DQ output hold time total from DQS_t, DQS_c (DBI-Disabled)	min(tQSH, tQSL)	-	min(tQSH, tQSL)	-	min(tQSH, tQSL)	-	min(tQSH, tQSL)	-	UI	
tQW	DQ output window time total, per pin (DBI-Disabled)	0.75	-	0.73	-	0.7	-	0.7	-	UI	3
tQW_dj	DQ output window time deterministic, per pin (DBI-Disabled)	TBD	-	TBD	-	TBD	-	TBD	-	UI	2,3
tDQSQ_DBI	DQS_t, DQS_c to DQ Skew total, per group, per access (DBI-Enabled)	-	0.18	-	0.18	-	0.18	-	0.18	UI	6
tQH_DB I	DQ output hold time total from DQS_t, DQS_c (DBI-Enabled)	Min (tQSH_DBI, tQSL_DBI)	-	Min (tQSH_DBI, tQSL_DBI)	-	Min (tQSH_DBI, tQSL_DBI)	-	Min (tQSH_DBI, tQSL_DBI)	TBD	UI	
tQW_total_DB I	DQ output window time total, per pin (DBI-Enabled)	0.75	-	0.73	-	0.7	-	0.7	-	UI	3
Data Strobe Timing											
tQSL	DQS, DQS# differential output low time (DBI-Disabled)	tCL(abs) -0.05	-	tCL(abs) -0.05	-	tCL(abs) -0.05	-	tCL(abs) -0.05	-	tCK(avg)	3,4
tQSH	DQS, DQS# differential output high time (DBI-Disabled)	tCH(abs) -0.05	-	tCH(abs) -0.05	-	tCH(abs) -0.05	-	tCH(abs) -0.05	-	tCK(avg)	3,5
tQSL_DB I	DQS, DQS# differential output low time (DBI-Enabled)	tCL(abs) -0.045	-	tCL(abs) -0.045	-	tCL(abs) -0.045	-	tCL(abs) -0.045	-	tCK(avg)	4,6
tQSH_DB I	DQS, DQS# differential output high time (DBI-Enabled)	tCH(abs) -0.045	-	tCH(abs) -0.045	-	tCH(abs) -0.045	-	tCH(abs) -0.045	-	tCK(avg)	5,6
a. The following Rx voltage and absolute timing requirements apply for DQ operating frequencies at or below 1333 for all speed											

Note:

- 1 The deterministic component of the total timing. Measurement method tbd.
- 2 This parameter will be characterized and guaranteed by design.
- 3 This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) -0.04.
- 4 tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as it measured the next rising edge from an arbitrary falling edge.
- 5 tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as it measured the next rising edge from an arbitrary falling edge.
- 6 This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) -0.04.

8.6 DQ Rx Voltage and Timing

The DQ input receiver mask for voltage and timing is shown [Figure 31](#) is applied per pin. The "total" mask (VdIVW_total, TdIVW_total) defines the area the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal with a BER of lower than tbd. The mask is a receiver property and it is not the valid data-eye.

Figure 31 - DQ Receiver(Rx) Mask

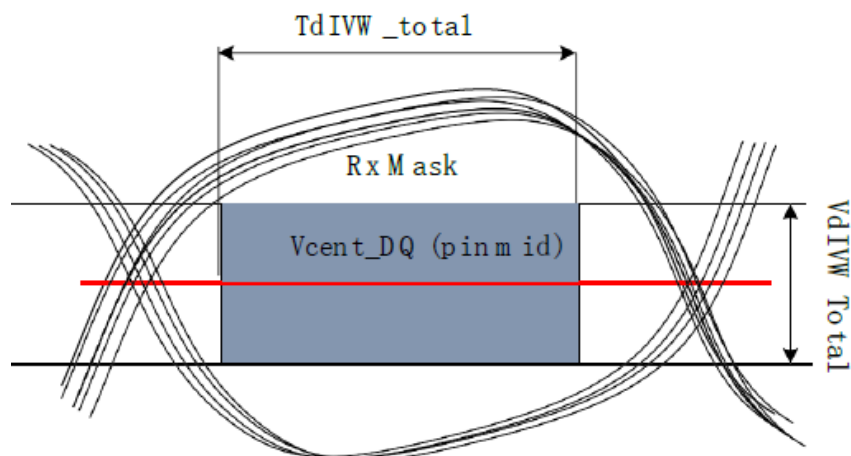
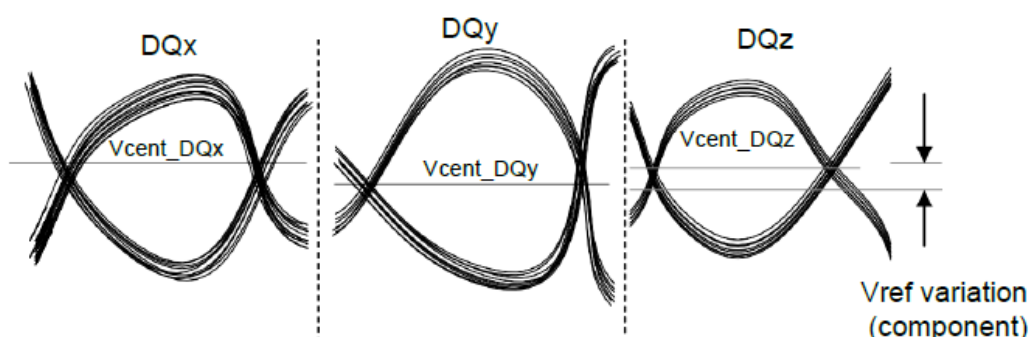
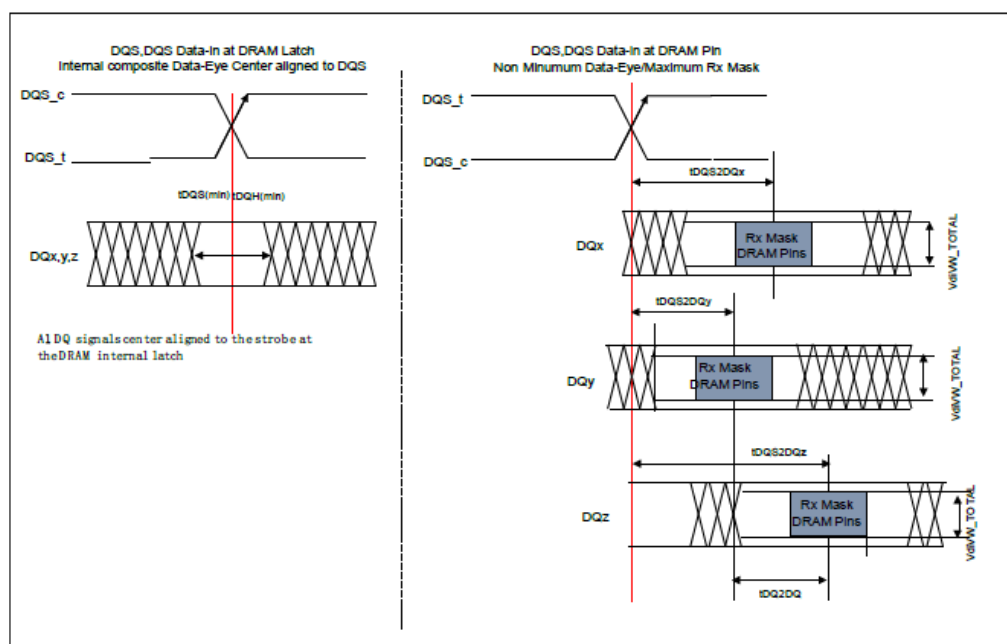


Figure 32 - Across Pin Vref DQ Voltage Variation



Vcent_DQ(pin_mid) is defined as the midpoint between the largest Vcent_DQ voltage level and the smallest Vcent_DQ voltage level across all DQ pins for a given DRAM component. Each DQVcent is defined by the center, i.e., widest opening, of the cumulative data input eye as depicted in Figure 32. This clarifies that any DRAM component level variation must be accounted for within the DRAM Rx mask. The component level Vref will be set by the system to account for Ron and ODT settings.

Figure 33 - DQ to DQS tDQS2DQ and tDQ2DQ Timings at the DRAM Pins Referenced from the Internal Latch

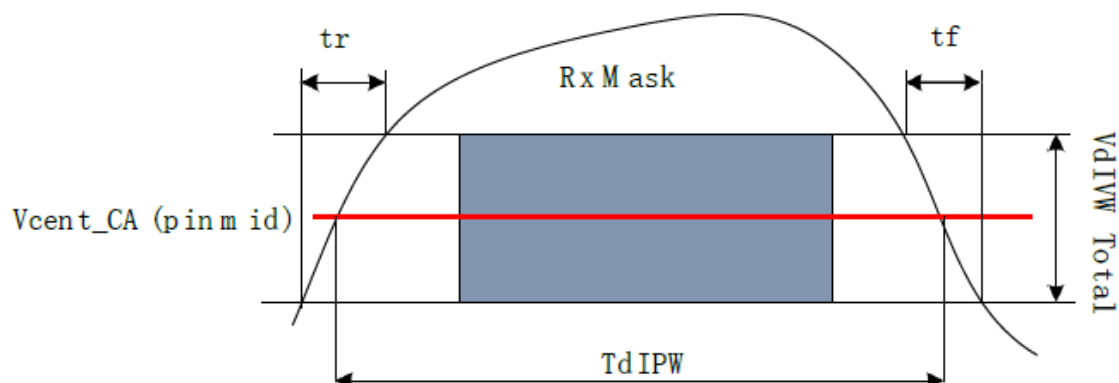


Note:

- 1 The tDQS2DQ is measured at the center (midpoint) of the TdiVW window.

- 2 The DQz represents the max tDQS2DQ in this example
- 3 DQy represents the min tDQS2DQ in this example

Figure 34 - DQ TdIPW and SRIN_dIVW Definition (for Each Input Pulse)



Note:

SRIN_dIVW=VdIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.

Figure 35 - DQ VIH_L_AC definition (for Each Input Pulse)

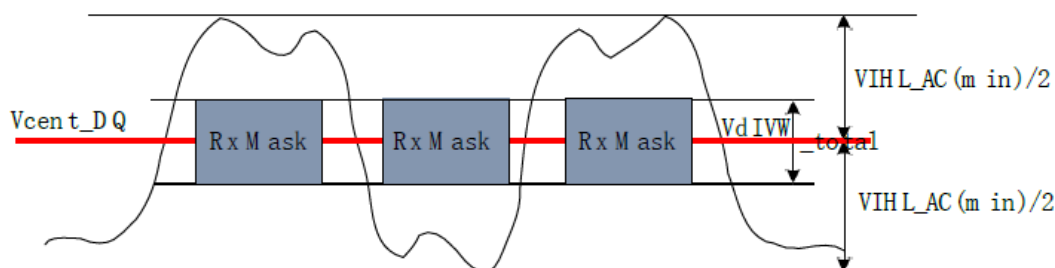


Table 44 - DRAM DQs in Receive Mode

Symbol	Parameter	DQ-		DQ-3200		DQ-4266		Unit	Note
		Min	Max	Min	Max	Min	Max		
VdIVW_total	Rx Mask voltage - p-p total	-	140	-	140	-	120	mV	1,2,3,4
TdIVW_total	Rx timing window total (At VdIVW voltage levels)	-	0.22	-	0.25	-	0.25	UI	1,2,4
TdIVW_1bit	Rx timing window 1 bit toggle (At VdIVW voltage levels)	-	TBD	-	TBD	-	TBD	UI	1,2,4,12
VIHL_AC	DQ AC input pulse amplitude pk-pk	180	-	180	-	170	-	UI	5,13
TdIPW DQ	Input pulse width (At VdIVW voltage levels)	0.45	-	0.45	-	0.45	-	UI	6
tDQS2DQ	DQ to DQS offset	200	800	200	800	200	800	ps	7
tDQ2DQ	DQ to DQ offset	-	30	-	30	-	30	ps	8
tQSL	tDQS2DQ_temp DQ to DQS offset temperature	-	0.6	-	0.6	-	0.6	ps/°C	9
tDQS2DQ_volt	DQ to DQS offset voltage variation	-	33	-	33	-	33	ps/50mV	10
SRIN_dIVW	Input Slew Rate over VdIVW_total	1	7	1	7	1	7	V/ns	11
tDQS2DQ_rank2rank	DQ to DQS offset rank to rank variation	-	200	-	200	-	200	ps	14,15,16

* UI=tCK(avg)min/2

- a. The Rx voltage and absolute timing requirements apply for all DQ operating frequencies at or below 1600 for all speed bins. For example $TdIVW_total(ps) = 137.5ps$ at or below 1600 operating frequencies

Note:

- 1 The Data Rx mask voltage and timing parameters are applied per pin and includes the DRAM DQ to DQS voltage AC noise impact for frequencies >20 MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC operating conditions.
- 2 The design specification is a BER <TBD. The BER will be characterized and extrapolated if necessary using a dual dirac method.
- 3 Rx mask voltage $VdIVW_total(max)$ must be centered around $Vcent_DQ(pin_mid)$.
- 4 $Vcent_DQ$ must be within the adjustment range of the DQ internal $Vref$.
- 5 DQ only input pulse amplitude into the receiver must meet or exceed VIH AC at any point over the total UI. No timing requirement above level. VIH AC is the peak to peak voltage centered around $Vcent_DQ(pin_mid)$ such that $VIHL_AC/2$ min must be met both above and below $Vcent_DQ$.
- 6 DQ only minimum input pulse width defined at the $Vcent_DQ(pin_mid)$.
- 7 DQ to DQS offset is within byte from DRAM pin to DRAM internal latch. Includes all DRAM process, voltage and temperature variation.
- 8 DQ to DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
- 9 TDQS2DQ max delay variation as a function of temperature.
- 10 TDQS2DQ max delay variation as a function of the DC voltage variation for VDDQ and VDD2. It includes the VDDQ and VDD2 AC noise impact for frequencies > 20MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package. For tester measurement $VDDQ = VDD2$ is assumed.
- 11 Input slew rate over $VdIVW$ Mask centered at $Vcent_DQ(pin_mid)$.
- 12 Rx mask defined for a one pin toggling with other DQ signals in a steady state.
- 13 VIH AC does not have to be met when no transitions are occurring.
- 14 The same voltage and temperature are applied to $tDQS2DQ_rank2rank$.
- 15 $tDQS2DQ_rank2rank$ parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.
- 16 $tDQS2DQ_rank2rank$ support was added to JESD209-4B, some older devices designed to support JESD209- 4 and JESD209-4A may not support this parameter. Refer to vendor datasheet.

9 AC Timing Parameters

9.1 Core AC Timing

Table 45 - Core AC Timing Table

Parameter	Symbol	Min/Max	Data Rate	Unit
Core Parameters			533/1066/1600/2133/2667/ 3200/3733/4267	
ACTIVATE-to-ACTIVATE command period (same bank)	tRC	MIN	tRAS + tRPab (with all bank precharge) tRAS + tRPpb (with per bank precharge)	ns
Minimum Self Refresh Time (Entry to Exit)	tSR	MIN	max(15ns, 3nCK)	ns
Self Refresh exit to next valid command delay	tXSR	MIN	max(tRFCab + 7.5ns, 2nCK)	ns
Exit Power-Down to next valid command delay	tXP	MIN	max(7.5ns, 5nCK)	ns
CAS-to-CAS delay	tCCD	MIN	8	tCK(avg)
Internal READ to PRECHARGE command delay	tRTP	MIN	max(7.5ns, 8nCK)	ns

RAS-to-CAS delay	tRCD	MIN	max(18ns, 4nCK)	ns
Row precharge time (single bank)	tRPpb	MIN	max(18ns, 4nCK)	ns
Row precharge time (all banks)	tRPab	MIN	max(21ns, 4nCK)	ns
Row active time	tRAS	MAX	max(42ns, 3nCK)	ns
Row active time	tRAS	MIN	Min(9 * tREFI * Refresh Rate, 70.2) us (Refresh Rate is specified by MR4, OP[2:0])	us
WRITE recovery time	tWR	MIN	max(18ns, 6nCK)	ns
WRITE-to-READ delay	tWTR	MIN	max(10ns, 8nCK)	ns
Active bank-A to active bank-B ¹	tRRD	MIN	max(10ns, 4nCK)	Max(7.5ns, 4nCK) ²
Precharge to Precharge Delay	tPPD	MIN	4	4
Four-bank ACTIVATE window	tFAW	MIN	40	30 ²

9.2 Read AC Timing

Table 46 - Read AC Timing Table

Parameter	Symbol	Min/Max	Data Rate	Unit
Core Parameters			533/1066/1600/2133/2667/3200/3733/4267	
READ preamble	tRPRE	MIN	1.8	tCK(avg)
0.5 tCK READ postamble	tRPST	MIN	0.4	tCK(avg)
1.5 tCK READ postamble	tRPST	MIN	1.4	tCK(avg)
DQ low-impedance time from CK_t, CK_c	tLZ(DQ)	MIN	(RL x tCK) + tDQSCK(Min) - 200ps	ps
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	MAX	(RL x tCK) + tDQSCK(Max) + tDQSQ(Max) + (BL/2 x tCK) - 100ps	ps
DQS_c low-impedance time from CK_t, CK_c	tLZ(DQS)	MIN	(RL x tCK) + tDQSCK(Min) - (tRPRE(Max) x tCK) - 200ps	ps
DQS_c high impedance time from CK_t, CK_c	tHZ(DQS)	MAX	(RL x tCK) + tDQSCK(Max) + (BL/2 x tCK) + (RPST(Max) x tCK) - 100ps	ps
DQS-DQ skew	tDQSQ	MAX	0.18	UI

9.3 tDQSCK Timing

Table 47 - tDQSCK Timing Table

Parameter	Symbol	Min	Max	Unit	Note
DQS Output Access Time from CK_t/CK_c	tDQSCK	1.5	3.5	ns	1
DQS Output Access Time from CK_t/CK_c -Temperature Variation	tDQSCK_temp	-	4	ps/°C	2
DQS Output Access Time from CK_t/CK_c -Voltage Variation	tDQSCK_volt	-	7	ps/mV	3

Note:

- 1 Includes DRAM process, voltage and temperature variation. It includes the AC noise impact for frequencies > 20 MHz and max voltage of 45 mV pk-pk from DC-20 MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC Operating conditions.
- 2 tDQSCK_temp max delay variation as a function of Temperature.
- 3 tDQSCK_volt max delay variation as a function of DC voltage variation for VDDQ and VDD2. tDQSCK_volt should be used to calculate timing variation due to VDDQ and VDD2 noise < 20 MHz. Host controller do not need to account for any variation due to VDDQ and VDD2 noise > 20 MHz. The voltage supply noise must comply to the component Min-Max DC Operating conditions. The voltage variation is defined as the Max[abs{tDQSCKmin@V1-

$t_{DQSCKmax@V2}$, $\text{abs}\{t_{DQSCKmax@V1}-t_{DQSCKmin@V2}\}/\text{abs}\{V1-V2\}$. For tester measurement $VDDQ = VDD2$ is assumed.

Table 48 - CK to DQS Rank to Rank Timing Table

Parameter	Symbol	Min/Max	Data Rate	Unit	Note
Read Timing			1600/1866/2133/2667/3200/4267		
CK to DQS Rank to Rank variation	$t_{DQSCK_rank2rank}$	Max	1.0	ns	1,2

Note:

- 1 The same voltage and temperature are applied to $t_{DQSCK_rank2rank}$.
- 2 $t_{DQSCK_rank2rank}$ parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.

9.4 Write AC Timing

Table 49 - Write AC Timing Table

Parameter	Symbol	Min/Max	Data Rate	Unit
Write Timing			533/1066/1600/2133/2667/3200/3733/4267	
Write command to 1st DQS latching	t_{DQSS}	Min Max	0.75 1.25	tCK(avg)
DQS input high-level	t_{DQSH}	Min	0.4	tCK(avg)
DQS input low-level width	t_{DQSL}	Min	0.4	tCK(avg)
DQS falling edge to CK setup time	t_{DSS}	Min	0.2	tCK(avg)
DQS falling edge hold time from CK	t_{DSH}	Min	0.2	tCK(avg)
Write preamble	t_{WPPE}	Min	1.8	tCK(avg)
0.5 tCK Write postamble	t_{WPST}^1	Min	0.4	tCK(avg)
1.5 tCK Write postamble	t_{WPST}^1	Min	1.4	tCK(avg)

Note:

The length of Write Postamble depends on MR3 OP1 setting.

9.5 Self Refresh Timing

Table 50 - Self Refresh AC Timing Table

Parameter	Symbol	Min/Max	Data Rate	Unit	Note
			533/1066/1600/2133/2667/3200/3733/4267		
Self Refresh Timing					
Delay from SRE command to CKE Input low	t_{ESCKE}	Min	Max(1.75ns, 3tCK)	ns	1
Minimum Self Refresh Time	t_{SR}	Min	Max(15ns, 3tCK)	ns	1
Exit Self Refresh to Valid commands	t_{XSR}	Min	Max($t_{RFCab} + 7.5\text{ns}$, 2tCK)	ns	2

Note:

Delay time has to satisfy both analog time(ns) and clock count(tCK). It means that t_{ESCKE} will not expire until CK has

toggled through at least 3 full cycles (3 *tCK) and 1.75ns has transpired.

9.6 Mode Register Read/Write AC Timing

Table 51 - Mode Register Read/Write AC Timing Table

Parameter	Symbol	Min/Max	Data Rate	Unit
Mode Register Read/Write Timing				
Additional time after tXP has expired until MRR command may be issued	tMRRi	Min	tRCD + 3nCK	-
MODE REGISTER READ command period	tMRR	Min	8	nCK
MODE REGISTER WRITE command period	tMRW	Min	MAX(10ns,10nCK)	-
Mode register set command delay	tMRD	Min	max(14ns,10nCK)	-

9.7 VRCG Enable/Disable Timing

Table 52 - VRCG Enable/Disable Timing Table

Speed		533/1066/1600/2133/2667/3200/3733/4267Mbps		Unit
Parameter	Symbol	Min	Max	
VREF high current mode enable time	tVRCG_ENABLE	-	200	ns
VREF high current mode disable time	tVRCG_DISABLE	-	100	

9.8 Command Bus Training AC Timing

Table 53 - Command Bus Training AC Timing Table

Parameter	Symbol	Min/Max	Data Rate	Unit
			533/1066/1600/2133/2667/3200/3733/4267	
Command Bus Training Timing				
Valid Clock Requirement after CKE Input low	tCKELCK	Min	Max(5ns, 5nCK)	-
Data Setup for VREF Training Mode	tDStrain	Min	2	ns
Data Hold for VREF Training Mode	tDHtrain	Min	2	ns
Asynchronous Data Read	tADR	Max	20	ns
CA Bus Training Command to CA Bus Training Command Delay	tCACD ²	Min	RU(tADR/tCK)	tCK
Valid Strobe Requirement before CKE Low	tDQSCKE ¹	Min	10	ns
First CA Bus Training Command Following CKE Low	tCAENT	Min	250	ns
VREF Step Time– multiple steps	tVREFCA_LONG	Max	250	ns
VREF Step Time– one step	tVREFCA_SHORT	Max	80	ns
Valid Clock Requirement before CS High	tCKPRECS	Min	2tck + tXP (tXP = max(7.5ns, 5nCK))	-
Valid Clock Requirement after CS High	tCKPSTCS	Min	max(7.5ns, 5nCK))	-
Minimum delay from CS to DQS toggle in command bus	tCS_VREF	Min	2	tCK

training				
Minimum delay from CKE High to Strobe High Impedance	tCKEHDQS	Min	10	ns
Valid Clock Requirement before CKE Input High	tCKCKEH	Min	Max(1.75ns, 3nCK)	-
CA Bus Training CKE High to DQ Tri-state	tMRZ	Min	1.5	ns
ODT turn-on Latency from CKE	tCKELODTon	Min	20	ns
ODT turn-off Latency from CKE	tCKELODToff	Min	20	ns
Exit Command Bus Training Mode to next valid command delay ³	tXCBT_Short	Min	Max(5nCK, 200ns)	-
	tXCBT_Middle	Min	Max(5nCK, 200ns)	-
	tXCBT_Long	Min	Max(5nCK, 250ns)	-

Note:

- 1 DQS_t has to retain a low level during tDQSCKE period, as well as DQS_c has to retain a high level.
- 2 If tCACD is violated, the data for samples which violate tCACD will not be available, except for the last sample (where tCACD after this sample is met). Valid data for the last sample will be available after tADR.
- 3 Exit Command Bus Training Mode to next valid command delay Time depends on value of VREF(CA) setting: MR12 OP[5:0] and VREF(CA) Range: MR12 OP[6] of FSP-OP 0 and 1. The details are shown in Table 61. Additionally exit Command Bus Training Mode to next valid command delay Time may affect VREF(DQ) setting. Settling time of VREF(DQ) level is same as VREF(CA) level.

Table 54 - Command Bus Training AC Timing Table for Mode 1

Parameter	Symbol	Min/Max	Data Rate	Unit	Note
			533/1066/1600/2133/2667/3200/3733/4267		
Command Bus Training Timing					
Clock and Command Validafter CKE Low	tCKELCK	Min	max(7.5ns, 3nCK)	tCK	
Asynchronous Data Read	tADR	Max	20	ns	
CA Bus Training Command to CA Bus Training Com- mand Delay	tCACD	Min	RU(tADR/tCK)	tCK	1
First CA Bus Training Com- mand Following CKE Low	tCAENT	Min	250	ns	
Valid Clock Requirement before CS High	tCKPRECS	Min	2tCK + tXP (tXP = max(7.5ns, 5nCK))		
Valid Clock Requirement after CS High	tCKPSTCS	Min	max(7.5ns, 5nCK))		
Clock and Command Validbefore CKE High	tCKCKEH	Min	2	tCK	
CA Bus Training CKE High to DQ Tri-state	tMRZ	Min	1.5	ns	
ODT turn-on Latency from CKE	tCKELODTon	Min	20	ns	
ODT turn-off Latency from CKE	tCKELODToff	Min	20	ns	
Exit Command Bus Training Mode to next valid com- mand delay	tXCBT_Short	Min	Max(5nCK, 200ns)		2
	tXCBT_Middle	Min	Max(5nCK, 200ns)		2

	tXCBT_Long	Min	Max(5nCK, 250ns)		2
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Note:

- 1 If tCACD is violated, the data for samples which violate tCACD will not be available, except for the last sample (where tCACD after this sample is met). Valid data for the last sample will be available after tADR.
- 2 Exit Command Bus Training Mode to next valid command delay Time depends on value of VREF(CA) setting: MR12 OP[5:0] and VREF(CA) Range: MR12 OP[6] of FSP-OP 0 and 1. Additionally exit Command Bus Training Mode to next valid command delay Time may affect VREF(DQ) setting. Settling time of VREF(DQ) level is same as VREF(CA) level.

Table 55 - Command Bus Training AC Timing Table for Mode 2

Parameter	Symbol	Min/Max	Data Rate	Unit	Note
			533/1066/1600/2133/2667/3200/3733/4267		
Command Bus Training Timing					
Valid Clock Requirement after CKE Input low	tCKELCK	Min	Max(5ns,5nCK)	ns	
Valid Clock Requirement before CS High	tCKPRECS	Min	2tCK + tXP (tXP = max(7.5ns, 5nCK))	-	
Valid Clock Requirement after CS High	tCKPSTCS	Min	max(7.5ns, 5nCK))	-	
Valid Strobe Requirement before CKE Low	tDQSCKE	Min	10	ns	1
First CA Bus Training Command Following CKE Low	tCAENT	Min	250	ns	
VREF Step Time - Long	tVREFCA_Long	Max	250	ns	2
VREF Step Time - Middle	tVREFCA_Mid-dle	Max	200	ns	3
VREF Step Time - Short	tVREFCA_Short	Max	100	ns	4
Data Setup for Vref Training Mode	tDStrain	Min	2	ns	
Data Hold for Vref Training Mode	tDHtrain	Min	2	ns	
Asynchronous Data Read Valid Window	tADVW	Min	16	ns	
		Max	80	ns	
DQS Input period at CBT mode	tDQSICYC	Min	5	ns	
		Max	100	ns	
Asynchronous Data Read	tADR	Max	20	ns	
DQS_c high impedance time from CS High	tHZCBT	Min	0	ns	
Asynchronous Data Read to DQ7 toggle	tAD2DQ7	Min	3	ns	
		Max	10	ns	
DQ7sample hold time	tDQ7SH	Min	10	ns	
		Max	60	ns	
Asynchronous Data Read Pulse Width	tADSPW	Min	3	ns	
		Max	10	ns	
Hi-Z to asynchronous Vref-CA valid data	tHZ2VREF	Min	Max(10ns, 5nCK)	-	
Read to Write Delay at CBT mode	tCBTRTW	Min	2	ns	
CA Bus Training Command to CA Bus Training Command Delay	tCACD	Min	Max(110ns, 4nCK)		
Minimum delay from CKE High to Strobe High Impedance	tCKEHDQS	Min	10	ns	
Clock and Command Valid before CKE High	tCKCKEH	Min	Max(1.75ns,3nCK)		
ODT turn-on Latency from CKE	tCKELODTon	Max	20	ns	
ODT turn-off Latency from CKE for ODT_CA	tCKELODToff	Max	20	ns	
ODT turn-off Latency from CKE for ODT_DQ and DOS	tCKEHODToff	Max	20	ns	

Parameter	Symbol	Min/Max	Data Rate	Unit	Note
			533/1066/1600/2133/2667/3200/3733/4267		
Command Bus Training Timing					
ODT_DQ turn-off Latency from CS high during CB Training	tODToffCBT	Max	20	ns	
ODT_DQ turn-on Latency from the end of Valid Data out	tODTonCBT	Max	Max(10ns, 5nCK)		
Exit Command Bus Training Mode to next valid command delay	tXCBT_Short	Min	Max(5nCK, 200ns)		5
	tXCBT_Middle	Min	Max(5nCK, 200ns)		5
	tXCBT_Long	Min	Max(5nCK, 250ns)		5

Note:

- 1 DQS_t has to retain a low level during tDQSCKE period, as well as DQS_c has to retain a high level.
- 2 VREFCA_Long is the time including up to VREFmin to VREFmax or VREFmax to VREFmin change across the VREFDQ Range in VREF voltage.
- 3 VREF_Middle is at least 2 stepsizes increment/decrement change within the same VREFDQ range in VREF voltage.
- 4 VREF_Short is for a single stepsize increment/decrement change in VREF voltage.
- 5 Exit Command Bus Training Mode to next valid command delay Time depends on value of VREF(CA) setting: MR12 OP[5:0] and VREF(CA) Range: MR12 OP[6] of FSP-OP 0 and 1.

9.9 Frequency Set Point Timing

Table 56 - Frequency Set Point Timing Table

Parameter	Symbol	Min/Max	Data Rate	Unit
			533/1066/1600/2133/2667/3200/3733/4267	
Frequency Set Point parameters				
Frequency Set Point Switching Time	tFC_Short ¹	Min	200	ns
Minimum Self Refresh Time	tFC_Middle ¹	Min	200	ns
Exit Self Refresh to Valid commands	tFC_Long ¹	Min	250	ns
Valid Clock Requirement after Entering FSP Change	tCKFSPE	Min	max(7.5ns, 4nCK)	-
Valid Clock Requirement before 1st Valid Command after FSP change	tCKFSPX	Min	max(7.5ns, 4nCK)	-

Note:

Frequency Set Point Switching Time depends on value of VREF(CA) setting: MR12 OP[5:0] and VREF(CA) Range: MR12 OP[6] of FSP-OP 0 and 1. Additionally change of Frequency Set Point may affect VREF(DQ) setting. Settling time of VREF(DQ) level is same as VREF(CA) level.

9.10 Write Leveling Timing

Table 57 - Write Leveling Timing Table

Parameter	Symbol	Min/Max	Value	Unit
DQS_t/DQS_c delay after write leveling mode is programmed	tWLDQSEN	Min	20	tCK
		Max	-	

Write preamble for Write Leveling	tWLWPRE	Min	20	tCK
		Max	-	
First DQS_t/DQS_c edge after write leveling mode is programmed	tWLMRD	Min	40	tCK
		Max	-	
Write leveling output delay	tWLO	Min	0	ns
		Max	20	
Mode register set command delay	tMRD	Min	max(14ns, 10nCK)	ns
		Max	-	
Valid Clock Requirement before DQS Toggle	tCKPRDQS	Min	max(7.5ns, 4nCK)	-
		Max	-	
Valid Clock Requirement after DQS Toggle	tCKPSTDQS	Min	max(7.5ns, 4nCK)	-
		Max	-	

Table 58 - Write Leveling Setup and Hold Time

Parameter	Symbol	Min/Max	Data Rate				Unit
			1600	2400	3200	4266	
Write Leveling Parameters							
Parameters Write leveling hold time	tWLH	Min	150	100	75	50	ps
Write leveling setup time	tWLS	Min	150	100	75	50	ps
Write leveling input valid window	tWLIVW	Min	240	160	120	90	ps

9.11 MPC [Write FIFO] AC Timing

Table 59 - MPC [Write FIFO] AC Timing Table

Parameter	Symbol	Min/Max	Data Rate
			533/1066/1600/2133/2667/3200/3733/4267
MPC Write FIFO Timing			
Additional time after tXP has expired until MPC [Write FIFO] command may be issued	tMPCWR	Min	tRCD + 3nCK

9.12 DQS Interval Oscillator AC Timing

Table 60 - DQS Interval Oscillator AC Timing Table

Parameter	Symbol	Min/Max	Value	Unit
Delay time from OSC stop to Mode Register Readout	tOSCO	Min	Max(40ns, 8nCK)	ns

Note:

Start DQS OSC command is prohibited until tOSCO(Min) is satisfied.

9.13 Read Preamble Training Timing

Table 61 - Read Preamble Training Timing Table

Parameter	Symbol	Min	Max
Delay from MRW command to DQS Driven	tSDO	-	Min(12nCK, 20ns)

9.14 ZQ Calibration Timing

Table 62 - ZQCal Timing Table

Parameter	Symbol	Min /Max	Value	Unit
ZQ Calibration Time	tZQCAL	Min	1	us
ZQ Calibration Latch Time	tZQLAT	Min	max(30ns,8nCK)	ns
ZQ Calibration Reset Time	tZQRESET	Min	max(50ns,3nCK)	ns

9.15 ODT CA AC Timing

Table 63 - ODT CA AC Timing Table

Speed		600/1866/2133/2400/3200/4266	
Parameter	Symbol	MIN	MAX
ODT CA Value Update Time	tODTUP	RU(TBDns/tCK(avg))	-

9.16 Power-Down AC Timing

Table 64 - Power-Down AC Timing

Parameter	Symbol	Min/Max	Data Rate	Unit	Note
			533/1066/1600/2133 /2667/3200/3733/4267		
Power Down Timing					
CKE minimum pulse width (HIGH and LOW pulse width) tCKE	tCKE	Min	Max(7.5ns,4nCK)	-	
Delay from valid command to CKE input LOW	tCMDCKE	Min	Max(1.75ns,3nCK)	ns	1
Valid Clock Requirement after CKE Input low	tCKELCK	Min	Max(5ns,5nCK)	ns	1
Valid CS Requirement before CKE Input Low	tCSCKE	Min	1.75	ns	
Valid CS Requirement after CKE Input low	tCKELCS	Min	Max(5ns,5nCK)	ns	
Valid Clock Requirement before CKE Input High	tCKCKEH	Min	Max(1.75ns,3nCK)	ns	1
Exit power- down to next valid command delay	tXP	Min	Max(7.5ns,5nCK)	ns	1
Valid CS Requirement before CKE Input High	tCSCKEH	Min	1.75	ns	
Valid CS Requirement after CKE Input High	tCKEHCS	Min	Max(7.5ns,5nCK)	ns	
Valid Clock and CS Requirement after CKE Input low after MRW Command	tMRWCKEL	Min	Max(14ns,10nCK)	ns	1
Valid Clock and CS Requirement after CKE Input low after ZQ Calibration Start Command	tZQCKE	Min	Max(1.75ns,3nCK)	ns	1

Note: Delay time has to satisfy both analog time(ns) and clock count(nCK).

10 Product Type Nomenclature

For reference the UnilC SDRAM component nomenclature is enclosed in this chapter.

Table 65 - Examples for Nomenclature Fields

LPDDR4 SDRAM	Field Number										
	1	2	3	4	5	6	7	8	9	10	11
	SC	B	11	R	16	32	2	C	F	–	04Z

Table 66 - LPDDR4 Memory Nomenclature

Field	Description	Values	Coding
1	UnilC Component Prefix	SC	UnilC Identifier
2	Product Group	B	Commodity chip
3	Interface Voltage [V]	11	1.1V
4	DRAM Technology	R	LPDDR4X
5	Component Density [Gbit]	16G	16Gbit
6	Number of I/Os	32	× 32
7	Die Number	2	2 die
8	Die Revision	C	Third
9	Package, Lead-Free Status	F	FBGA, lead-free
11	Power	–	Standard power product
		L	Low power product
	Speed Grade	04Z	LPDDR4-4266
		03A	LPDDR4-3733

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